ANALYSIS AND DESIGN OF A POWER SWITCHED-CAPACITOR DC-DC VOLTAGE CONVERTER

By

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KEY TO SYMBOLS

The unit system in this paper is SI (MKS). Unless otherwise specified, the convention used in this dissertation is as follows:

x^*	Instantaneous value of the variable x
x	Low-frequency component of x^*
$\hat{x}$	Small-signal perturbation of x^*
X	Average value of x

The nomenclature used is as follows:

a	A constant
a_1	A first-order coefficient matrix for the Taylor series expansion of the A matrix around the steady-state value of the duty cycle
a_{11}	A term in the a_1 matrix
a_{12}	A term in the a_1 matrix
a_2	A second-order coefficient matrix for the Taylor series expansion of the A matrix around the steady-state value of the duty cycle
a_{21}	A term in the a_1 matrix
a_{22}	A term in the a_1 matrix
A	Averaged state-space matrix for the switching interval
A_0	The gain relating the output voltage to the reference voltage at dc
A_1	State-space matrix for the charge interval
A_{11}	A term of the averaged state-space matrix A

A_{12}	A term of the averaged state-space matrix A
A_2	State-space matrix for the discharge interval
A_{21}	A term of the averaged state-space matrix A
A_{22}	A term of the averaged state-space matrix A
A_{CL}	The gain relating the output voltage to the reference voltage
A_{amp}	The open-loop gain of the operational amplifier used in the compensation circuit
A_d	The drain area of a MOSFET
A_{dnorm}	The drain area of a MOSFET normalized by the drain current
A_θ	Cross-sectional area of a piece of material used for heat transfer
b_1	A first-order coefficient matrix for the Taylor series expansion of the B matrix around the steady-state value of the duty cycle
b_{11}	A term in the b_1 matrix
b_{11}	A term in the b_1 matrix
b_2	A second-order coefficient matrix for the Taylor series expansion of the B matrix around the steady-state value of the duty cycle
b_{21}	A term in the b_1 matrix
b_{22}	A term in the b_1 matrix
B	Averaged state-space matrix for the switching interval
B_1	State-space matrix for the charge interval
B_{11}	A term of the averaged state-space matrix B
B_{12}	A term of the averaged state-space matrix B

B_2	State-space matrix for the discharge interval
B_{21}	A term of the averaged state-space matrix B
B_{22}	A term of the averaged state-space matrix B
C	Value of charging capacitors C_2, C_3,... C_n
C_1	Output capacitor
C_{dg}	The drain-gate capacitance of a MOSFET
C_{dgo}	The zero-bias drain-gate capacitance of a MOSFET
C_{ds}	The drain-source capacitance of a MOSFET
C_{f1}	A capacitor used in the compensation network
C_{f2}	A capacitor used in the compensation network
C_{gs}	The gate-source capacitance of a MOSFET
C_{gso}	The zero-bias gate-source capacitance of a MOSFET
C_{iss}	MOSFET input capacitance, as specified on the manufacturer's data sheets
C_j	Charging capacitors C_2, C_3,... C_n
C_{min}	Minimum allowable value of C for a given design
C_o	The gate oxide capacitance of a MOSFET
C_{oss}	MOSFET output capacitance, as specified on the manufacturer's data sheets
C_p	Parasitic capacitance of a switching device
C_{rss}	MOSFET reverse transfer capacitance, as specified on the manufacturer's data sheets
C_T	The total capacitance in a converter, $C_1 + C_2 + ...C_n$

C_{Tmin}	The minimum total capacitance needed by a particular design
C_x	The sum of the gate-source and the drain-source capacitances of a MOSFET
C_y	The sum of the drain-gate and the drain-source capacitances of a MOSFET
d	Charging duty cycle
d'	1-d
D_{jA}	Diodes that conduct during the charge interval
D_{jB}	Diodes that conduct during the discharge interval
E	Energy
E_{cgd}	Energy lost by the drain-gate capacitor of M_C during a charge-discharge cycle
E_{csd}	Energy lost by the drain-source capacitor of M_C during a charge-discharge cycle
E_{csg}	Energy lost by the gate-source capacitor of M_C during a charge-discharge cycle
E_{jmdg}	Energy lost by the drain-gate capacitor of M_j during a charge-discharge cycle
E_{jmds}	Energy lost by the drain-source capacitor of M_j during a charge-discharge cycle
E_{jmgs}	Energy lost by the gate-source capacitor of M_j during a charge-discharge cycle
E_{jA}	Energy lost by the capacitance of D_{jA} during a charge-discharge cycle
E_{jB}	Energy lost by the capacitance of D_{jB} during a charge-discharge cycle
E_s	Total energy switching loss during a switching period
f	Frequency
f_s	Switching frequency
f_{smax}	Maximum allowable switching frequency
g	An arbitrary function

g_m	Transconductance of M_C
G_c	The open-loop input current to output voltage transfer function
G_d	The open-loop duty cycle to output voltage transfer function
G_{gate}	The transfer function from the input of the gate-drive circuit to the drain current of M_C
H_c	The compensation network used to adjust the phase margin of the closed-loop system
H_{gate}	The gain of the gate-drive circuit of M_C
H_{pwm}	The gain of the pulse-width modulator in the feedback network
i	Integer index, $i = 1, 2, \ldots n$
i_{C1}	The current through C_1
i_{Cj}	The current through C_2-C_n
i_{cs}	The current source value in the state-space averaged equivalent circuit
i_d	Drain current of a MOSFET
i_{diode}	The current through a diode
i_{Mc}	The current through M_C
i_{Mj}	The current through M_2-M_n
i_o	The output current through R_L
i_s	Source current of a MOSFET
I	Identity matrix
I_{dmax}	Maximum diode current

I_{gd}	The current capability of the gate-drive circuit of M_2-M_n
I_{loss}	Average charging current loss during the charge interval
I_{Mcmax}	The current rating of M_C
I_{max}	The minimum of I_{Mjmax} and I_{dmax}
I_{on}	The current through M_C during the charge interval
I_{rating}	The current rating of M_j
j	Integer index, $j = 2, 3, \ldots n$
k	The value of C_1 is kC
k_c	A constant
k_T	A constant
K	The ratio of ω_{co} to ω_z or the ratio of ω_p to ω_{co}
K_m	The conductance parameter of a MOSFET
L	The channel length of a MOSFET
m	An integer value
M	The voltage stepdown ratio, V_{in} / V_o
M_C	MOSFET acting as a current-source
M_j	Switching MOSFETs $M_2, M_3, \ldots M_n$
n	Number of stages
n_{max}	Maximum number of stages that can be used for a given converter design
n_{min}	Minimum number of stages that can be used for a given converter design
p	A constant

P	A transformation matrix relating the state variables from the beginning to the end of the charge interval
P_c	Average conduction power dissipated by a component
P_{cA}	Average conduction power dissipated by each charge diode D_{2A}-D_{nA}
P_{cB}	Average conduction power dissipated by each discharge diode D_{2B}-D_{nB}
P_{cC1}	Average conduction power dissipated by C_1
P_{cC}	Average conduction power dissipated by each C_2-C_n
P_{cm}	Average conduction power dissipated by each M_2-M_n
P_{cmc}	Average conduction power dissipated by M_C
P_{in}	Average input power
P_{jsm}	Average switching power loss in each M_2-M_n
P_{jtA}	Average total power loss in each charge diode D_{2A}-D_{nA}
P_{jtB}	Average total power loss in each discharge diode D_{2B}-D_{nB}
P_{jtm}	Average total power loss in each M_2-M_n
P_o	Average output power
P_{omax}	The maximum output power available from a converter
P_{Ri}	Average power dissipated by R_i, a resistor in the compensation circuit
P_s	Total average switching power loss
P_{smc}	Average switching power loss of M_C
P_t	Average total power dissipated by a component
P_{tC}	Average total power dissipated by each C_2-C_n

P_{tC1}	Average total power dissipated by M_C
P_{tmax}	The maximum power a device can dissipate at a given temperature
P_{tmc}	Average total power dissipated by M_C
q	Integer index, $q = 0, 1, \ldots \infty$
Q	The rate at which heat energy is transferred by conduction from a body at temperature T_1 to another body at temperature T_2
Q_g	The charge needed to bring the gate of a MOSFET from zero to some voltage
r_{eq}	The ac resistance value in the averaged state-space equivalent circuit
R_1	Equivalent series resistance of C_1
R_D	The drift resistance of the epidrain bulk region of a MOSFET
R_L	Load resistance
R_b	One of the input resistors used in the compensation circuit
R_{eq}	The dc resistance value in the averaged state-space equivalent circuit
R_{esr}	Equivalent series resistance of C_2-C_n
R_f	The feedback resistor used in the compensation circuit
R_i	One of the input resistors used in the compensation network
R_{on}	"On" resistance of M_j
R_{onmax}	Maximum allowable "on" resistance of M_j
R_{onmin}	Minimum allowable "on" resistance of M_j
R_{onp}	"On" resistance of the current source in the state-space averaged equivalent circuit

R_θ	Thermal resistance of a piece of material
$R_{\theta cs}$	Thermal resistance of the case of a MOSFET or diode to a heat sink
$R_{\theta jc}$	Thermal resistance of the junction of a MOSFET or diode to its case
$R_{\theta sa}$	Thermal resistance of a heat sink to air
s	The Laplace variable
S	Capacitance per unit volume
S_m	The safety margin for V_{block} and V_{wk}
t	Time
t_{max}	Time where peak output ripple occurs, referenced from the beginning of the discharge interval
t_s	The time it takes for M_2-M_n to switch states from on to off or vice versa
T	Switching period, inverse of switching frequency
T_1	A constant temperature
T_2	A constant temperature
T_a	Ambient temperature
T_j	The junction temperature of a MOSFET or diode
T_{jmax}	The maximum junction temperature rating of a MOSFET or diode
T_{CL}	Loop-gain
u	Input vector
v	Voltage
v_{C1}	Voltage of C_1

v_{Cj}	Voltage of C_2, C_3,...C_n
v_{Cjmax}	Maximum allowable voltage of C_2, C_3,...C_n for a given design
v_c	The output voltage of the compensation circuit H_c
v_d	Drain voltage of a MOSFET
v_{dg}	Drain-gate voltage of a MOSFET
v_{drain}	The drain voltage of M_C
v_{ds}	Drain-source voltage of a MOSFET
v_F	Diode "on" voltage
v_g	Gate voltage of a MOSFET
v_{gs}	Gate-source voltage of a MOSFET
v_{in}	Input voltage
v_{inv}	The voltage at the inverting terminal of the operational amplifier used in the compensation network
v_o	Output voltage
v_{ref}	The reference voltage used to set the value of output voltage in the closed-loop system
v_s	Source voltage of a MOSFET
v_{sat}	The limiting velocity for electrons in silicon
V_T	MOSFET threshold voltage
V_{block}	MOSFET or diode blocking voltage
V_{CT}	Volume of the total capacitance C_T

V_{dmax}	The maximum allowable drain voltage on M_C to keep it in saturation
V_{dsat}	Minimum voltage across a MOSFET to keep it in saturation
V_{gate}	The gate voltage of M_C needed for the drain current to equal I_{on}
V_{gsp}	The voltage where the V_{gs}-Q_g curve of a MOSFET plateaus
V_{inmin}	The minimum allowable input voltage to keep M_C in saturation
V_{jB}	The cathode voltage of D_{jB} at the end of the charge interval
V_{jM}	The drain voltage of M_j at the end of the charge interval
V_{lin}	The gate-source voltage of M_j necessary to assure operation in the linear region during the discharge interval
V_{omax}	The maximum allowable output voltage
V_{wk}	Working voltage rating of a capacitor
W	Channel width of a MOSFET
x	State-space vector over the switching period
x_m	Sampled data points of x^* at $t = mT$
x_{m+1}	Sample data points of x^* at $t = (m+1)T$
x_{m+d}	Sample data points of x^* at $t = (m+d)T$
Y_1	A constant
Y_2	A constant
Y_{gate}	The gate voltage to drain current transfer function of a p-channel MOSFET
Z_f	The feedback impedance of the compensation network
Z_i	The open-loop, small-signal input impedance of the converter

Z_{ic}	The closed-loop, small-signal input impedance of the converter
Z_o	The open-loop, small-signal output impedance of the converter
Z_{oc}	The closed-loop, small-signal output impedance of the converter
Z_{ps}	Impedance of the converter power stage equivalent circuit
α	Ratio of C_1 to $C_1+C_2+...C_n$
β	The MOSFET transconductance parameter
δ	The thickness of a piece of material used to conduct heat
ΔV_C	The change in voltage of a charging capacitor during the charge interval
ΔV_o	Output voltage ripple
$\Delta\varepsilon_{A0}$	The percent maximum error in the gain equation relating v_o and v_{ref}
$\Delta\eta$	The difference between the maximum possible efficiency and the minimum acceptable efficiency
ε_A	The error term in the gain equation relating v_o and v_{ref}
ε_{A0}	The error term in the gain equation relating v_o and v_{ref} at dc
ϕ_m	The phase margin of the loop-gain T_{CL}
Φ	A constant
η	Converter efficiency
η_{max}	The maximum possible efficiency available from a given converter
γ	A constant
Γ	A constant
Γ_1	A constant

Γ_2	A constant
λ_1	Eigenvalue of matrix A_1
λ_{2a}	Eigenvalue of matrix A_2
λ_{2b}	Eigenvalue of matrix A_2
μ	A constant
μ_p	The hole mobility in the inversion layer of a MOSFET
ρ_θ	Thermal resistivity of a material
σ	A constant
τ	A time constant
τ_1	A time constant, the inverse of λ_1
τ_{2a}	A time constant, the inverse of λ_{2a}
τ_{2b}	A time constant, the inverse of λ_{2b}
θ	A constant
ω_c	The zero in the open-loop input current to output voltage transfer function
ω_{co}	The cutoff frequency where the magnitude of T_{CL} equals one
ω_d	The zero in the open-loop duty cycle to output voltage transfer function
ω_p	The pole frequency of the compensation network
ω_z	The zero frequency of the compensation network
Ψ	Ratio of the average charging current through C_1-C_n to I_{on} during the charge interval

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Major Department: Electrical and Computer Engineering

Switched-mode voltage converter circuits that utilize capacitors as the energy transfer element are called switched-capacitor voltage converters. Switched-capacitor voltage converters are attractive because they use no magnetic components and may one day be amenable to monolithic integration.

Previous attempts at analyzing switched-capacitor voltage converters have relied on a technique called State-Space-Averaging. While this technique is acceptable for converters having natural frequencies much less than the switching frequency (linear ripple), its accuracy suffers when this assumption is not true. This dissertation focuses on a specific switched-capacitor topology that has nonlinear ripple, and uses a new technique to aid in the analysis and design. This new technique, called Modified State-Space-Averaging, is generally suitable for analysis of voltage converters with nonlinear ripple.

In this dissertation, Modified State-Space-Averaging is used along with practical

approximations to derive the steady-state operating conditions of the converter. The effect of switching losses on the steady-state output voltage is also accounted for, and a method of calculating these losses is given.

Modified State-Space-Averaging is also used to derive the open-loop dynamic response of the converter, and a method of feedback compensation is presented to control the closed-loop frequency response. The dynamic analysis also leads to the derivation of continuous-time equivalent circuits that model the transient and frequency responses of the converter, allowing much shorter simulation times.

An optimized design procedure is presented that allows a converter to be designed for minimum volume for given values of input voltage, output voltage, efficiency, and output ripple. The performance limits of the converter, such as maximum output power, maximum efficiency, and minimum capacitance are presented in graphical form.

Experimental circuits are used to show that a switched-capacitor dc-dc converter can process up to several tens of watts of output power at an efficiency exceeding 80%. Experimental and simulation verification of the steady-state and dynamic analysis is given.

CHAPTER 1

INTRODUCTION

Power supplies are an integral part of today's electronic systems. Their function is to provide a regulated dc voltage source to the various electronic components in the system. Initially, linear power supplies were used, but they suffered from low efficiency (30 to 60%) and required large 60 Hz transformers to step down the input line voltage. Large capacitors were necessary to filter the dc output voltage, and a transistor operated in the active region (low efficiency) was used to provide output regulation [34]. Today, high efficiency switched-mode supplies use magnetic energy transfer and solid-state switches to convert one dc voltage to another. Although much progress has been made in reducing the size of the magnetic components used in such supplies [1][18][35][37][54], these components remain a barrier to monolithic integration.

On the other hand, it has been shown that capacitors have fewer physical barriers to monolithic integration than do magnetic components [8][24][26][45]. As capacitor technology develops towards full integration, it is possible that they could be used in an integrated switched-mode supply as the energy transfer element. Switched-mode dc-dc converter circuits that utilize capacitors as the energy transfer element are called Switched-Capacitor Dc-Dc Converters (SCDDCs). Commercially available SCDDCs include the ICL7660 [12] and the LT1054 [25]. However, these products offer a limited range of voltage conversion and operate at very low power levels.

This dissertation focuses on a specific stepdown SCDDC topology, with a four-stage converter shown in its simplified form in Fig. 1-1. As will be discussed in Chapter 2, the capacitors C_2-C_4 are charged in series and discharged in parallel, while C_1 acts as a filter for the load resistor R_L. During the charge interval, the switches labeled S_c are closed and the switches labeled S_d are open. During the discharge interval, the switches labeled S_d are closed and the switches labeled S_c are open.

Previous attempts at analyzing SCDDCs [6][7][28][29][49][52] have relied on State-Space-Averaging (SSA) [33], and have been limited to an output power of a few watts or less. It has been shown [52] that the efficiency of a SCDDC can exceed 80% by proper choice of the capacitive step-down ratio. Thus, the power rating of a SCDDC does not have to be restricted to a "low" power rating of a few watts, and a "medium" power rating of several tens of watts is conceivable. In the practical case, however, the analysis and design results [52] are not directly applicable since, as shown in Fig. 1-2, the assumption of linear ripple [33] does not hold. Other analysis techniques derived from SSA can be found [9][53], but these techniques also rely on the assumption that the natural frequencies of the system are much less than the switching frequency. Therefore, general analysis and design methods for the SCDDC need to be revisited.

This dissertation presents a new technique for analyzing a switched-capacitor dc-dc converter. This technique, called Modified State-Space-Averaging (MSSA) [17], is generally suitable for analysis of converters with nonlinear ripple. Like SSA, the results from MSSA are used to derive the steady-state operation and the dynamic response of the

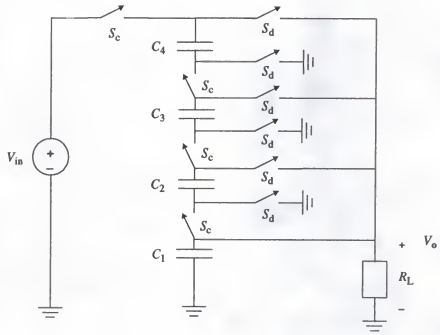


Figure 1-1. Four-stage switched-capacitor dc-dc converter.

converter. Results from the steady-state analysis lead to expressions for output voltage, output ripple, charging capacitor voltage, and efficiency. Results from the dynamic analysis can be used to design a method for optimizing the response of the closed-loop system and to derive a non-switching equivalent circuit that models the transient and frequency responses of the converter. The remainder of the dissertation is as follows.

Chapter 2 presents the circuit topology and discusses the switching operation of a SCDDC. Two methods of control, input current and duty ratio, are given. Equivalent circuits for both the charge and discharge intervals are presented, along with justification for the inclusion of the switching losses in the state-space equations.

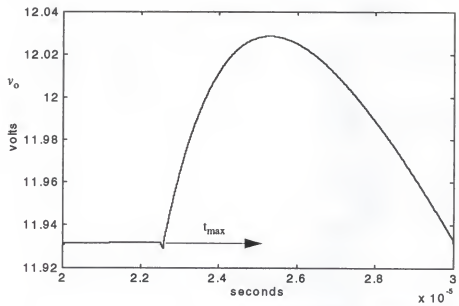


Figure 1-2. Output voltage ripple for a four-stage, 48 W SCDDC with f_s = 100 KHz, PSPICE simulation.

Chapter 3 introduces the analysis problem by giving the background for State-Space-Averaging, and provides the justification for Modified State-Space-Averaging. A numerical example is given to give a comparision between the two. Practical approximations are made, allowing the analysis results to be simplified into a usable format. These approximations allow the derivation of the steady-state operating conditions, and calculation of the values of steady-state output voltage, output ripple, charging capacitor voltage, and efficiency.

Chapter 4 analyzes the power dissipation (conduction and switching) in the SCDDC and uses basic thermal analysis to determine if a device is operating within its maximum ratings.

Chapter 5 uses the averaged state-space equation derived from MSSA to obtain the open-loop transfer functions and impedances, along with the large-signal and small-signal continuous-time equivalent circuits for the converter [33]. These equivalent circuits provide a reduction in the time needed to simulate a converter circuit. Because its switching operation, PSPICE simulation [32] of a SCDDC can take several minutes to several hours, depending on the number of stages and the speed of the computer. This chapter also looks at the effect of the feedback loop on the transfer functions, impedances, and output voltage of the converter. Analysis and modification of the closed-loop gain allows the designer to set the frequency response of the system. An example is given to show how to implement the feedback loop in a closed-loop converter.

Chapter 6 presents a design procedure based on analysis results derived from Modified State-Space-Averaging. The procedure gives the smallest total capacitance (and size) for the set of input parameters of output voltage, output power, output voltage ripple and efficiency. Standard parameter models of currently available MOSFETs, diodes, and capacitors used in the procedure are given. These models calculate the device parameters that would be found in a datasheet, all as functions of input voltage and output power.

Chapter 7 presents the performance limits of the SCDDC in graphical form using the component models given in Chapter 6. In this chapter, the minimum possible input voltage, the maximum possible efficiency, and the maximum possible output power are all plotted as a functions of the input design parameters. The design procedure in Chapter 6 is

then used to obtain curves for the minimum total capacitance used and the total capacitance volume of the SCDDC as a function of the input design parameters.

Chapter 8 presents design examples, and compares analytical, simulation and experimental results. In this chapter, the analysis results of the preceding chapters are verified using simulation and experimental data. Design examples are presented for three medium-power converters, and experimental circuits similar to the design examples are fabricated to show that high-efficiency, medium-power converters are feasible. Experimental data is shown to closely agree with analysis and simulation results. Simulation data showing the effect of switching losses on the output voltage at switching frequencies of 100 KHz and 1 MHz is given. Good agreement between calculated and simulated values is shown, excepted as noted.

Chapter 9 summarizes the main contributions and accomplishments of this dissertation, and suggests topics for further research.

CHAPTER 2

CIRCUIT TOPOLOGY AND OPERATION

This chapter introduces the topology for the switched-capacitor step-down dc-dc converter, and discusses switching operation. Equivalent circuits are given to simplify the analysis presented in the next chapter. Section 2.1 introduces the function of the circuit components in a switched-capacitor step-down dc-dc converter. Section 2.2 discusses the switching operation of the converter, and presents equivalent circuits for the charge and discharge intervals. Section 2.3 discusses the necessary conditions for the current source to remain in the saturation region of operation. Section 2.4 justifies the inclusion of the switching losses in the state-space equations.

2.1. Introduction

As shown in Figs. 1-1 and 2-1, a SCDDC generally consists of n stages. The first stage consists of capacitor C_1, which acts as a filter for the load resistor R_L. Each of the other stages consists of a capacitor C_j, diodes D_{jA} and D_{jB}, and a MOSFET M_j. MOSFET M_C operates as a current source that controls the output voltage. It is shown as a p-channel device because they can be driven with simpler gate-drive circuitry, as compared to an n-channel device. The other MOSFETs and the diodes are used as switches. As will be shown later in Chapter 3, the output voltage can also be controlled by the duty ratio of the input current.

2.2. Switching Operation

Each switching period T consists of a charge interval dT ($mT < t < (m+d)T$), and a discharge interval $d'T$ ($(m+d)T < t < (m+1)T$). At the beginning of the charge interval, M_2-M_4 and D_{2B}-D_{4B} are off, and M_C and D_{2A}-D_{4A} are turned on, charging the capacitors C_1-C_4. The charge circuit is shown in Fig. 2-2(a). During the discharge interval M_C and D_{2A}-D_{4A} are off, and M_2-M_4 and D_{2B}-D_{4B} are turned on, discharging C_2-C_4 into C_1 and R_L. The discharge circuit is shown in Fig. 2-2(b).

Figures 1-2 and 2-3 show the typical waveforms of an SCDDC switched at 100 KHz and 0.25 duty ratio. It can be seen from Figs. 2-2(a), 2-3(a), and 2-3(b) that during the charge interval, the current I_{on} flows through M_C, C_1-C_4, and D_{2A}-D_{4A} and establishes a voltage at the drain of M_C which is the sum of the voltages across C_1-C_4 and D_{2A}-D_{4A}. During the discharge interval (Fig. 2-2(b)), C_2-C_4 discharges into C_1 and R_L through M_2-M_4. Note that in the discharge interval the current through M_4 (Fig. 2-3(c)) is exponential, not linear. The voltage ripple (Fig. 1-2) is also obviously nonlinear. These nonlinear waveforms necessitate the use of Modified State-Space-Averaging discussed in the next chapter.

The output voltage ripple shown in Fig. 1-2 is for $d = 1/n$, which corresponds to a zero slope for v_o during the charge interval. When $d < 1/n$, the slope of v_o during the charge interval is positive because $I_{on} > v_o/R_L$. When $d > 1/n$, the slope of v_o is negative during the charge interval because $I_{on} < v_o/R_L$.

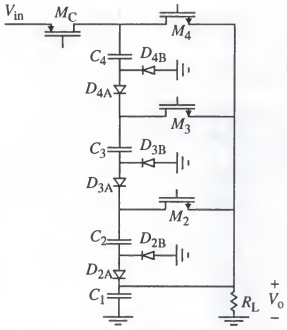


Figure 2-1. A four-stage step-down converter.

2.3. Current Source Operation

During the charge interval, M_C must remain in the saturation region; which means that the voltage across it must be greater than or equal to V_{dsat}, the saturation voltage. This gives rise to the condition

$$V_{in} \geq V_{dsat} + V_{C1}[(m+d)T] + (n-1)(V_F + I_{on}R_{esr} + V_{Cj}[(m+d)T]) \qquad (2\text{-}1)$$

where the equivalent-series-resistance (ESR) of C_1 has been neglected. The relationship between drain current and gate-source voltage for a p-channel power MOSFET is given by

$$i_d = K_m(-V_{gs} + V_T) \qquad (2\text{-}2)$$

where the threshold voltage V_T is a negative number. For most applications the power MOSFET will be operating in a region where there is a linear relationship between the drain current and the gate-source voltage, and the value for K_m is given by [2]

$$K_m = C_o W v_{sat} \tag{2-3}$$

where $v_{sat} \approx 8 \times 10^6$ cm / second [10].

If the MOSFET is operating in the region where there is a quadratic relationship between the drain current and the gate-source voltage, the value of K_m is given by [15]

$$K_m = \frac{W}{2L} C_o \mu_p (-V_{gs} + V_T) = \frac{\beta}{2}(-V_{gs} + V_T) \tag{2-4}$$

The manufacturer's data sheets usually contain a drain current vs. gate-source voltage plot that will allow a designer to determine which equation is valid for a specific application.

Therefore, for a power MOSFET operating in the linear region of drain current vs. gate-source voltage

$$V_{dsat} = \frac{I_{on}}{K_m} = \frac{I_{on}}{g_m} \tag{2-5}$$

where the transconductance g_m of M_C can be found in the manufacturer's data sheets. For a power MOSFET operating in the nonlinear region of drain current vs. gate-source voltage

$$V_{dsat} = \sqrt{\frac{2I_{on}}{\beta}} \tag{2-6}$$

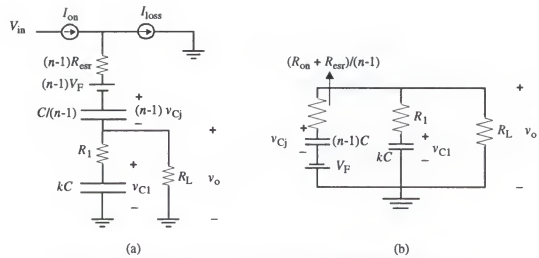


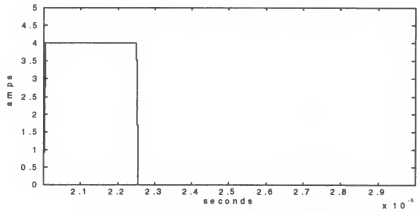
Figure 2-2. Equivalent circuits for the charge (a) and discharge (b) intervals.

It appears from (2-1) that to keep M_C in saturation, the right-hand side of (2-1) should be made as small as possible, e.g., by making n or $V_{Cj}[(m+d)T]$ small. It will be shown later, however, that n is directly proportional to the efficiency and $V_{Cj}[(m+d)T]$ inversely proportional to the size of the semiconductor devices and the capacitors. Thus, it is desirable to keep the right-hand side of (2-1) as close to V_{in} as possible.

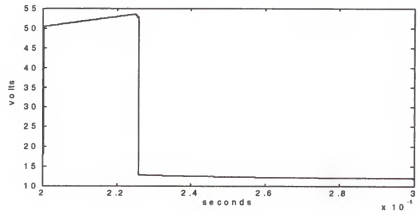
2.4. Switching Loss

In a real circuit the MOSFETs and diodes have parasitic capacitances that must be charged and discharged during switching. The charging and discharging of these capacitors results in switching losses [42][43], reducing the output power and thus the output voltage. It will be shown later that this is equivalent to having a net reduction of charging

(a)



(b)



(c)

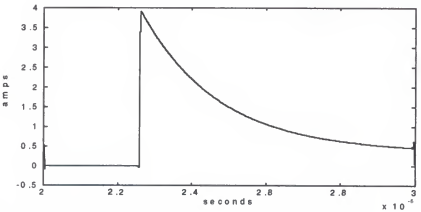


Figure 2-3. Current through M_C (a); the voltage at the drain of M_C (b); and current through M_4 (c); for an SCDDC with P_o = 48 W, V_{in} = 55 *V*, V_o = 12 V, n = 4, f_s = 100 KHz, I_{on} = 4 A, R_L = 3 Ω, C = 9.6 μF, R_{esr} = 3 mΩ, k = 9, R_{on}(25° *C*) = 0.3 Ω, V_F = 0.3 V, PSPICE simulation.

current through C_1-C_n. In Fig. 2(a), this reduction in current is shown as I_{loss}, which represents the average charging current loss over the charge interval. The average charging current during the charge interval is then given by

$$I_{on} - I_{loss} = \Psi I_{on} \tag{2-7}$$

where Ψ will be determined later from the switching power loss P_s and the output power P_o, or

$$\Psi = \sqrt{\frac{P_o}{P_o + P_s}} \tag{2-8}$$

Figure 2-4 shows the charging currents through M_C and C_2-C_4 at the beginning of the charge interval for a four-stage converter. The successive reduction in current is due to the switching currents flowing into the parasitic capacitances of the MOSFETs and diodes, as shown in Fig. 2.5.

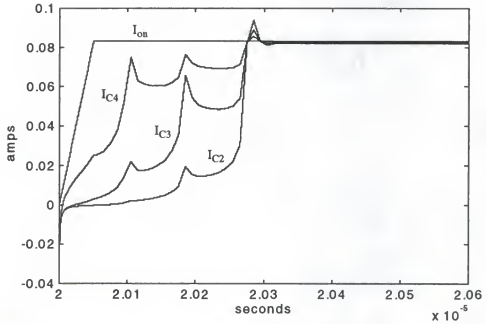


Figure 2-4. Charging currents through M_C and C_2-C_4 at the beginning of the charge interval for an SCDDC with P_o = 1 W, V_{in} = 55 V, V_o = 12 V, n = 4, I_{on} = 83 mA, R_L = 144 Ω, C = 80 nF, R_{esr} = 3 mΩ, k = 60, R_{on} = 0.3 Ω, V_F = 0.3 V, PSPICE simulation.

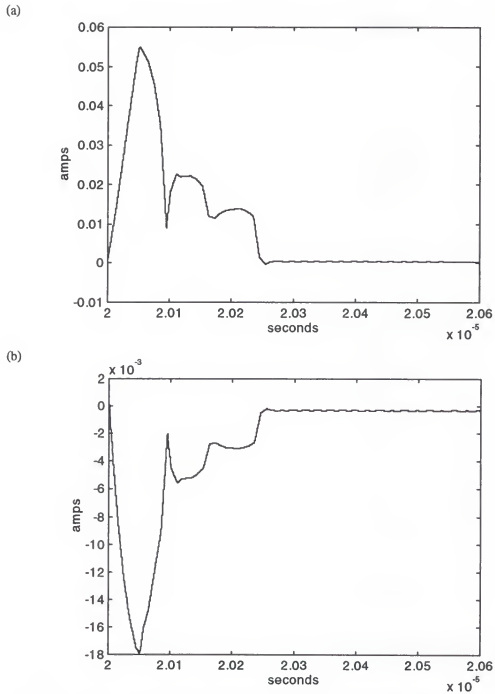


Figure 2-5. Switching currents through the drain of M_4 (a) and through D_{4B} (b) at the beginning of the charge interval for the circuit of Fig. 2-4, PSPICE simulation.

CHAPTER 3

MODIFIED STATE-SPACE-AVERAGING

This chapter presents the derivation of Modified State-Space-Averaging (MSSA), which is generally suited for the analysis of converters with nonlinear ripple. Section 3.1 introduces the analysis problem and discusses State-Space-Averaging, a previous method of analysis. Section 3.2 derives the state-space equations and gives justification for the use of Modified State-Space-Averaging. The averaged state-space equation over the switching period is derived from averaging the state-space equations of the charge and discharge intervals. Section 3.3 justifies the use of practical approximations, and simplifies the averaged state-space equation to a usable form. Section 3.4 uses the averaged state-space equation to analyze the SCDDC during steady-state operation. Expressions are given for the steady-state output voltage, output voltage ripple, and efficiency.

3.1. Introduction

In any switching power supply with a dc output voltage the instantaneous output voltage will vary with the switching frequency, a term normally called the output ripple. A designer is interested in being able to model the average value of the output voltage, which normally changes at a much lower frequency than the switching frequency. Figure 3-1 illustrates this problem by showing the output voltage for the circuit of Fig. 2-1 at start-up. Previous work [33][52] has relied on State-Space-Averaging to model this low frequency,

average output voltage. State-Space-Averaging is a technique which is based on the assumption that the natural frequencies of the circuit are much less than the switching frequency, which means that the instantaneous output voltage is linear over a switching interval (linear ripple). Mathematically, this means that the exponential terms in the solution for the instantaneous output voltage can be approximated as

$$e^{\frac{-t}{\tau}} \approx 1 - \frac{t}{\tau} \qquad t \ll \tau \tag{3-1}$$

However, it will be shown that when the circuit of Fig. 2-1 is designed using typical, commercially available components that (3-1) is not always valid. Therefore, a new technique had to be developed to account for the case where (3-1) is not true. This new technique, called Modified State-Space-Averaging, can generally be used for converters where the output ripple is nonlinear.

3.2. Modified State-Space-Averaging

This section presents the derivation of Modified State-Space-Averaging. Modified State-Space-Averaging seeks to model the slowly-varying "envelope" constructed from the regularly sampled points x_m derived from the instantaneous state vector $x^*(t)$. The frequent choices for x_m are $x^*(mT)$, the value of $x^*(t)$ at the beginning of each switching period [9], and $\langle x^*(t) \rangle_m$, the average of $x^*(t)$ over a switching period [33]. The various choices for x_m are related to each other by transformations. Since the ripple in an SCDDC is generally nonlinear, it is convenient to let the MSSA state variable be

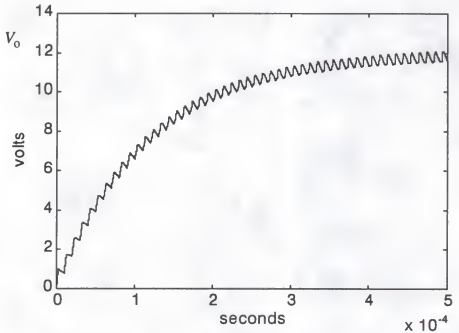


Figure 3-1. Output voltage at start-up for the circuit of Fig. 2-3, PSPICE simulation.

$$x_m = x^*(mT) \tag{3-2}$$

where

$$x^* = \begin{bmatrix} v_{C1}{}^* \\ v_{Cj}{}^* \end{bmatrix} \tag{3-3}$$

It is assumed that the voltages of C_2, C_3,...C_n are equal, thus allowing the simplification of an n-state system down to a 2-state system [52].

Modified State-Space-Averaging starts with the state-space equations of the equivalent circuits shown in Figs. 2-2(a) and 2-2(b). It is assumed that the circuit switches states in a time much shorter than the switching period, or

$$t_s \ll T \tag{3-4}$$

For the charge interval shown in Fig. 2-2(a):

$$x^* = A_1 x^* + B_1 u^* \tag{3-5}$$

where

$$A_1 = \begin{bmatrix} \frac{-1}{kCR_L} & 0 \\ 0 & 0 \end{bmatrix} \tag{3-6}$$

$$B_1 = \begin{bmatrix} \frac{1}{kC} & 0 \\ \frac{1}{C} & 0 \end{bmatrix} \tag{3-7}$$

$$u^* = \begin{bmatrix} i_{Mc} \\ v_F \end{bmatrix} \tag{3-8}$$

For a constant input U where

$$U = \begin{bmatrix} I_{on} \\ V_F \end{bmatrix} \tag{3-9}$$

the solution to (3-5) is [22]

$$v_{C1}^*(t) = e^{\lambda_1(t-mT)} v_{C1}(mT) + \lambda_1^{-1}(e^{\lambda_1(t-mT)} - 1)\frac{\Psi I_{on}}{kC} \tag{3-10}$$

$$v_{Cj}^*(t) = v_{Cj}(mT) + \frac{\Psi I_{on}}{C}(t-mT) \tag{3-11}$$

where

$$\lambda_1 = \frac{1}{\tau_1} \approx \frac{-1}{kCR_L} \tag{3-12}$$

For the discharge interval shown in Fig 2-2(b):

$$\dot{x}^* = A_2 x^* + B_2 u^* \tag{3-13}$$

where

$$A_2 = \begin{bmatrix} \dfrac{-(n-1)}{kC((R_{on}+R_{esr}) \| R_L)} & \dfrac{(n-1)}{kC(R_{on}+R_{esr})} \\ \dfrac{1}{C(R_{on}+R_{esr})} & \dfrac{-1}{C(R_{on}+R_{esr})} \end{bmatrix} \tag{3-14}$$

$$B_2 = \begin{bmatrix} 0 & \dfrac{-(n-1)}{kC(R_{on}+R_{esr})} \\ 0 & \dfrac{1}{C(R_{on}+R_{esr})} \end{bmatrix} \tag{3-15}$$

For a constant input U, the solution of (3-13) is

$$x^*(t) = e^{A_2[t-(m+d)T]}x_{m+d} + A_2^{-1}(e^{A_2[t-(m+d)T]} - I)B_2U \tag{3-16}$$

where the exponential term involving A_2 has two natural time constants (second-order system) which will be designated as τ_{2a} and τ_{2b}.

Using (3-10), (3-11), and (3-16), the discrete derivative of the state can be approximated by the Euler approximation [20][22]

$$\dot{x}_m = \dot{x}(mT) \approx \frac{x_{m+1} - x_m}{T} \tag{3-17}$$

From (3-10) and (3-11), the boundary condition at $t = (m+d)T$ is

$$v_{C1}[(m+d)T] = v_{C1}(mT)e^{\frac{-dT}{kCR_L}} + \Psi I_{on}R_L\left(1 - e^{\frac{-dT}{kCR_L}}\right) \tag{3-18}$$

$$v_{Cj}[(m+d)T] = v_{Cj}(mT) + \frac{dT\Psi I_{on}}{C} \tag{3-19}$$

From (3-16), the boundary condition at $t = (m+1)T$ is

$$x_{m+1} = A_2e^{A_2d'T}x_{m+d} + A_2^{-1}(e^{A_2d'T} - I)B_2U \tag{3-20}$$

Use of (3-18), (3-19), and (3-20) in (3-17) allows the expression of x_{m+1} in terms of x_m.

Up to this point the procedure deriving Modified State-Space-Averaging is the same as that for State-Space-Averaging. In State-Space-Averaging the exponential terms in (3-18) and (3-20) are approximated as

$$e^{\frac{-dT}{kCR_L}} \approx 1 - \frac{dT}{kCR_L} \tag{3-21}$$

$$e^{A_2 d'T} \approx I + A_2 d'T \tag{3-22}$$

The result is that (3-17) can be cast in the following continuous state-space form:

$$\dot{x} = Ax + BU \tag{3-23}$$

where

$$A = dA_1 + d'A_2 \tag{3-24}$$

$$B = dB_1 + d'B_2 \tag{3-25}$$

However, in some cases (3-22) is not valid, and thus the need for Modified State-Space-Averaging. A "low" power converter has $\tau_{2b} << T$ and $\tau_{2a} >> T$. For these conditions, the exponential functions in (3-20) can be approximated as

$$e^{\frac{-d'T}{\tau_{2b}}} \approx 0 \tag{3-26}$$

$$e^{\frac{-d'T}{\tau_{2a}}} \approx 1 - \frac{d'T}{\tau_{2a}} \tag{3-27}$$

As the power increases to a "medium" level, τ_{2b} can become very close to T, because C must also increase. The condition that $\tau_{2a} >> T$ is still valid, and (3-27) still holds. The exponential function in (3-26) can no longer be approximated by zero, nor the first two or three terms in the series as in other forms of State-Space-Averaging [9][33]. Therefore, in Modified State-Space-Averaging, the exponential term containing τ_{2b} is carried along as a constant μ, where μ is defined as

$$\mu = e^{\frac{-d'T}{\tau_{2b}}} \tag{3-28}$$

Since $\tau_1 >> T$, the exponential term in (3-18) can be approximated as

$$e^{\frac{-dT}{\tau_1}} \approx 1 - \frac{dT}{kCR_L} = \sigma \tag{3-29}$$

This allows (3-10) and (3-11) to be rewritten in matrix form as

$$x_{m+d} = (I + dTA_1)x_m + dTB_1U \tag{3-30}$$

or

$$x_{m+d} = Nx_m + PU \tag{3-31}$$

where

$$N = \begin{bmatrix} \sigma & 0 \\ 0 & 1 \end{bmatrix} \qquad P = \begin{bmatrix} \frac{dT\Psi}{kC} & 0 \\ \frac{dT\Psi}{C} & 0 \end{bmatrix} \tag{3-32}$$

Thus, with Modified State-Space-Averaging (3-17) can be cast in the following continuous state-space form:

$$\dot{x} = Ax + BU \tag{3-33}$$

where A and B are functions of μ, and are given by

$$A = \begin{bmatrix} \sigma\theta - \gamma\sigma(n-1)C\left(R_L + \frac{R_{on} + R_{esr}}{n-1}\right) - \frac{1}{\Gamma} & \gamma(n-1)CR_L \\ \gamma\sigma kCR_L & \theta - \gamma kC(R_L + R_1) - \frac{1}{\Gamma} \end{bmatrix} \frac{\Gamma}{T} \tag{3-34}$$

$$B = \begin{bmatrix} \frac{d\Psi}{kC}\left[\theta - \gamma(n-1)C\left(R_L + \frac{R_{on} + R_{esr}}{n-1}\right) + \gamma(n-1)CR_L\right] & \frac{\gamma\Gamma(n-1)CR_L}{T} \\ \frac{d\Psi\Gamma}{C}(\theta - \gamma kC(R_L + R_1) + \gamma CR_L) & \frac{1 - \Gamma(\theta - \gamma kC(R_L + R_1))}{T} \end{bmatrix} \tag{3-35}$$

where

$$\theta = \tau_{2a} e^{\frac{-(1-d)T}{\tau_{2a}}} - \mu\tau_{2b} \tag{3-36}$$

$$\gamma = e^{\frac{-(1-d)T}{\tau_{2a}}} - \mu \tag{3-37}$$

$$\Gamma = \frac{1}{\tau_{2a} - \tau_{2b}} \tag{3-38}$$

$$\tau_{2a} = C[R_L(n-1+k) + R_{on} + R_{esr} + kR_1] \tag{3-39}$$

$$\tau_{2b} = \frac{kC[R_1(R_{on} + R_{esr}) + R_L(R_{on} + R_{esr}) + (n-1)R_1R_L]}{[R_L(n-1+k) + R_{on} + R_{esr} + kR_1]} \tag{3-40}$$

Table 3-1 shows the analysis results for the circuit of Fig. 2-3 for both SSA and MSSA. Notice that the output ripple is much greater using SSA as compared to MSSA. Because of this over-estimation of the output ripple, the design procedure presented in Chapter 6 will calculate more total capacitance than is actually needed for a specific design.

Table 3-1: A comparision of SSA and MSSA for the circuit of Fig. 2-3, PSPICE simulation.

Parameter	SSA	MSSA	PSPICE
$V_{C1}(mT)$	12.01 V	12.01 V	12.02 V
$V_{Cj}(mT)$	12.71 V	12.45 V	12.38
ΔV_o	144 mV	95.7 mV	93.4 mV

3.3. Practical Approximations

Because of the availability of MOSFETs with R_{on} less than 0.1 ohm [36], and multi-layer ceramic capacitors with R_{esr} ranging from a few milliohms to a few tenths of a milliohm [4][40], practical constraints were invoked to simplify the exact analytical results.

- $R_L >> (R_{on}+R_{esr}) >> R_1$
- For low ripple, $C_1 >> (C_2+C_3+...C_n)$

As stated previously, the nonlinear ripple is due to an exponential current spike sent to the output during the discharge interval, meaning that one of the eigenvalues of A_2 is on the order of the switching frequency. Under the stated assumptions, these eigenvalues are given by

$$\lambda_{2a} = \frac{1}{\tau_{2a}} \approx \frac{-1}{(k+n-1)R_L C} \tag{3-41}$$

$$\lambda_{2b} = \frac{1}{\tau_{2b}} \approx \frac{-1}{\alpha(R_{on}+R_{esr})C} \tag{3-42}$$

where

$$\alpha = \frac{k}{k+n-1} \tag{3-43}$$

The state matrices of (3-34)-(3-35) can also be rewritten as

$$A \approx \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} = \begin{bmatrix} -\left[\frac{T}{kCR_L} + (1-\mu)(1-\alpha)\sigma\right] & (1-\mu)(1-\alpha) \\ (1-\mu)\sigma\alpha & -(1-\mu)\alpha \end{bmatrix} \frac{1}{T} \tag{3-44}$$

$$B \approx \begin{bmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{d\Psi}{kC}[1+(1-\mu)(n-1)] & \dfrac{-(1-\mu)(n-1)}{kT} \\ \dfrac{d\Psi\mu}{C} & \dfrac{1-\mu}{T} \end{bmatrix} \tag{3-45}$$

3.4. Steady-State Solution

The steady-state capacitor voltages at the beginning of the charge interval can be found by setting the derivative in (3-33) equal to zero, which results in

$$X = -A^{-1}BU \tag{3-46}$$

Using (3-44)-(3-45), the steady-state capacitor voltages can be given as

$$V_{C1}(mT) \approx nd\Psi I_{on}R_L \tag{3-47}$$

$$V_{Cj}(mT) \approx V_{C1}(mT) + V_F + \mu d\Psi I_{on}\left(R_{on} + R_{esr} + \frac{d}{f_s C(1-\mu)}\right) \tag{3-48}$$

In the limit as C goes to infinity, the results in (3-47) and (3-48) can be shown to reduce to the state-space results [52].

A designer usually does not have much control over the $V_{C1}(mT)$ and V_F terms in (3-48) because, as shown later, $V_{C1}(mT) \approx V_o$ and V_F is the on-drop of the diodes. Therefore, if $V_{Cj}[(m+d)T]$ is to be kept small as dictated by (2-1) to keep M_C in saturation, the capacitive reactance $1/f_sC$ and the parasitic resistances (R_{on}+R_{esr}) need to be made

small. In particular, since I_{on} could be several amperes at medium power levels (e.g., 50 W), (R_{on}+R_{esr}) needs to be on the order of 1 Ω or less. Consequently, τ_{2b} defined in (3-42) is comparable to T, making the output waveform (Fig. 1-2) nonlinear and necessitating Modified State-Space-Averaging. One may argue that (R_{on}+R_{esr}) should be made as small as practically allowed so that the same $V_{Cj}[(m+d)T]$ can be achieved with a small value of C. However, there are several problems with this argument. First, practical capacitors are made such that a lower R_{esr} corresponds to a larger C. Secondly, a MOSFET with too small an R_{on} would be difficult to drive because of the large gate capacitance. Thirdly, if (R_{on}+R_{esr}) is so small that $\tau_{2b} << T$, C_2-C_n would discharge into C_1 in the form of exponential current spikes with high peak value, causing electromagnetic interference problems. Thus, it is recommended that if possible, R_{on} and C be selected such that

$$0.25d'T \le \tau_{2b} \le d'T \tag{3-49}$$

From (3-31), the voltage of C_1 at the beginning of the discharge interval is given by

$$V_{C1}[(m+d)T] = \sigma V_{C1}(mT) + \frac{dT\Psi I_{on}}{kC} \approx V_{C1}(mT)\left(\sigma + \frac{T}{n\tau_1}\right) \tag{3-50}$$

Under the assumption that $\tau_1 >> T$, (3-50) reduces to

$$V_{C1}[(m+d)T] \approx V_{C1}(mT) \tag{3-51}$$

The voltage of C_j at the beginning of the discharge interval is

$$V_{Cj}[(m+d)T] = V_{Cj}(mT) + \Delta V_C \tag{3-52}$$

where

$$\Delta V_C = \frac{dT\Psi I_{on}}{C} \tag{3-53}$$

Assuming that C_1 can be chosen so that R_1 is small enough to be neglected, the output voltage can be approximated as

$$v_o^* \approx v_{C1}^* \tag{3-54}$$

This gives the steady-state average output voltage as

$$V_o \approx V_{C1}(mT) \approx nd\Psi I_{on} R_L \tag{3-55}$$

The output voltage ripple is calculated from

$$\Delta V_o = \max(v_o^*) - \min(v_o^*) \tag{3-56}$$

There are two cases that must be considered in evaluating (3-56). For $d > 1/n$, (3-56) becomes

$$\Delta V_o = v_o^*[(m+d)T + t_{max}] - v_o^*[(m+d)T] \tag{3-57}$$

where t_{max} is shown in Fig. 1-2. For $d \leq 1/n$, (3-56) becomes

$$\Delta V_o = v_o^*[(m+d)T + t_{max}] - v_o^*(mT) \tag{3-58}$$

If (3-57) and (3-58) are plotted as a function of d, they will intersect at a minimum point where $d \approx 1/n$. Figure 3-2 shows a MATLAB [30] plot of (3-57) and (3-58) for the circuit of Fig. 1-2, where $n = 4$. The two equations intersect at a minimum ripple of $\Delta V_o = 0.097$ V at $d = 0.25$. In Chapter 7 the estimated value for ΔV_o will be shown to be 0.095 V.

For the minimum-ripple condition ($d = 1/n$), the value of ΔV_o is given by (3-58), which can be written using (3-54) as

$$\Delta V_o = v_{C1}^*[(m+d)T + t_{max}] - v_{C1}^*(mT) \tag{3-59}$$

Expansion of (3-16) gives v_{C1}^* during the discharge interval, and the value of t_{max} can be found from where the derivative of v_{C1}^* equals zero. Substitution of (3-16), (3-47)-(3-48), and (3-50)-(3-55) into (3-59) will result in the simplified equation:

$$\Delta V_o \approx \frac{dT\Psi I_{on}(1-\alpha)}{C}[1 - \Phi(1 - \ln\Phi)] \tag{3-60}$$

where

$$\Phi \approx \frac{\tau_{2b}}{T}\frac{n}{n-1} \tag{3-61}$$

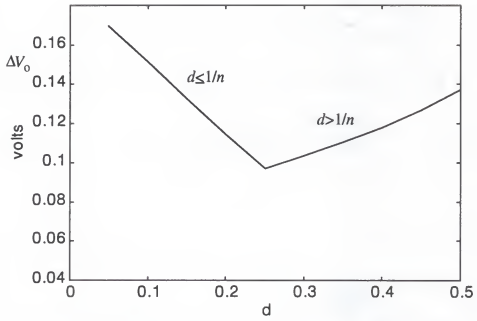


Figure 3-2. The output ripple as a function of duty cycle for $d > 1/n$ and $d \leq 1/n$ for the circuit of Figure 2-3.

A more complete derivation of (3-60) can be found in Appendix A. Figure 3-3 shows the variation of R_{on} and C with fixed ΔV_o for a typical four-stage converter.

The efficiency is calculated from

$$\eta = \frac{P_o}{P_i} = \frac{V_o^2}{R_L} \cdot \frac{1}{dI_{on}V_{in}} \tag{3-62}$$

which can be rewritten using (3-55) as

$$\eta = \frac{nV_o}{V_{in}}\Psi \cdot 100\% \tag{3-63}$$

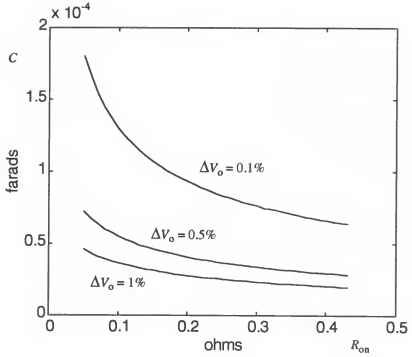


Figure 3-3. Charging capacitance vs. R_{on} for a converter with n =4, V_{in} = 50 V, V_o = 10 V, P_o = 50 W, C = 1.9 μF, k = 2, and f_s = 100 KHz.

The maximum possible efficiency obtainable from a given converter is when switching losses are negligible, or $\Psi = 1$. This gives the maximum efficiency as

$$\eta_{max} = \frac{nV_o}{V_{in}} \cdot 100\% \tag{3-64}$$

which is equal to the previously derived expression for efficiency [52].

CHAPTER 4

POWER DISSIPATION AND THERMAL ANALYSIS

Calculating the power dissipation in a device is necessary so that the proper heat sinking and mounting procedures can be used to keep the device operating well within its maximum ratings. Power dissipation in the SCDDC is due mainly to conduction losses. However, switching losses can also have significant effect on the performance of a SCDDC. As the switching frequency moves up into the 100 KHz range and beyond, switching losses can begin to cause a noticeable reduction in the output voltage. Switching losses occur when energy is lost in the parasitic capacitors of the MOSFETs and diodes as they charge and discharge [42].

This chapter analyzes the power loss in the SCDDC. Section 4.1 calculates the conduction loss of each component in the converter. Section 4.2 presents an analysis of the effects of switching losses on the output voltage of an SCDDC. An expression to calculate the energy lost during a charge-discharge cycle of a capacitor is derived, along with the power lost due to switching. Section 4.3 calculates the total power dissipated per component using the results from the previous two sections. Section 4.4 discusses heat flow in a material. The concept of thermal resistance is used to calculate the junction temperature of a device. This junction temperature is used in the design procedure to determine the size of the heat sink needed to keep the device operating within its rated conditions.

4.1. Conduction Losses

Conduction losses occur in an active device while the device is conducting current, as opposed to switching losses where power is lost as the device is switching from "on" to "off" or vice versa. In a passive component such as a resistor, losses occur when the component is conducting current. During the charge interval, conduction losses occur in M_C, D_{2A}-D_{nA}, and C_1-C_n. During the discharge interval, conduction losses occur in M_2-M_n, D_{2B}-D_{nB}, and C_1-C_n.

The conduction loss over a switching period can be calculated from the familiar

$$P_c = \frac{1}{T}\int_{mT}^{(m+1)T} v(t-mT)i(t-mT)dt \tag{4-1}$$

where v and i describe the time dependence of the voltage and current across the device.

Using (4-1), the loss in the current source M_C is given by

$$P_{cmc} \approx dI_{on}\left[V_{in} - V_o - (n-1)\left(V_F + V_{Cj}(mT) + \frac{\Delta V_C}{2}\right)\right] \tag{4-2}$$

The loss in each charge diode D_{2A}-D_{nA} is given by

$$P_{cA} \approx dI_{on}V_F \tag{4-3}$$

The loss in each discharge diode D_{2B}-D_{nB} is given by

$$P_{cB} \approx \frac{d'I_{on}V_F}{n-1} \tag{4-4}$$

The loss in each switching MOSFET M_2-M_n is given by

$$P_{cm} \approx \frac{d' I_{on}}{n-1}\left(V_{Cj}(mT) + \frac{\Delta V_C}{2} - V_o\right) \tag{4-5}$$

The loss in each capacitor C_2-C_n is given by

$$P_{cC} \approx (I_{on})^2 R_{esr}\left(d + \frac{d'}{(n-1)^2}\right) \tag{4-6}$$

Finally, the loss in capacitor C_1 is given by

$$P_{cC1} \approx R_1\left(d\left(I_{on} - \frac{V_o}{R_L}\right)^2 + 2d'\left(kC\frac{\Delta V_o}{t_{max}}\right)^2\right) \tag{4-7}$$

where t_{max} is given in (A-14).

Figure 4-1 shows the typical conduction loss of each component (as modeled in Chapter 6) for an eight-stage converter.

4.2. Switching Losses

As previously stated in Chapter 2, switching losses occur when the parasitic capacitors of the MOSFETs and diodes charge and discharge. The switching losses take away from the available output power, reducing the output voltage. In (3-55), this effect is shown to be equivalent to reducing the charging current from I_{on} to ΨI_{on}, as shown in Fig 2-2(a).

The MOSFET and diode capacitance model used is found in [43], and is given by

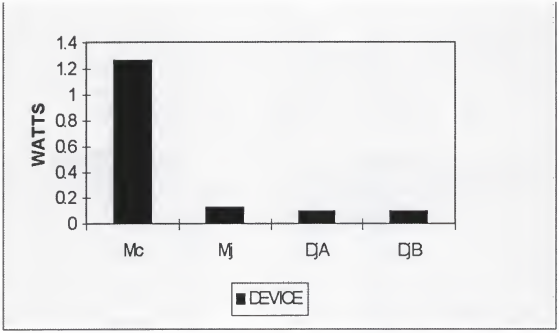


Figure 4-1. Conduction power loss in each component for a converter with n =8, V_{in} = 100 V, V_o = 10 V, P_o = 10 W, C = 1.9μF, k = 5, f_s = 207 KHz, ΔV_o = 1%.

$$C_p(v) = C_o\left(1 + \frac{v}{\phi}\right)^{-m} \tag{4-8}$$

where v is the voltage across C_p, C_o is the zero-bias capacitance, ϕ is the p-n potential and m is a constant.

The energy lost during a charge-discharge cycle of a voltage-dependent capacitor as it charges from a voltage of zero to a voltage of V is

$$E = 2\int_0^V vC_p(v)dv \tag{4-9}$$

which, for $m = 0.5$, simplifies to

$$E = \frac{4}{3}C_o\phi\left[\left(1+\frac{V}{\phi}\right)^{0.5}(V-2\phi)+2\phi\right] \tag{4-10}$$

For a capacitor whose value remains constant with voltage ($C_p(v) = C_o$), (4-9) simplifies to

$$E = C_o(V)^2 \tag{4-11}$$

4.2.1. Switching MOSFET Energy Loss

The capacitance model of a power MOSFET is made up of three capacitors, the voltage-dependent drain-gate and drain-source, and the constant gate-source [43]. During a switching cycle, the drain voltage of M_j goes from V_o to V_{jM} and back, the gate voltage goes from zero to V_o+V_{lin} and back, while the source voltage remains constant at V_o, where for $j = 2, 3,... n$,

$$V_{jM} = V_o + (j-1)V_F + (j-1)V_{Cj}[(m+d)T] \tag{4-12}$$

Thus, the energy absorbed by the drain-gate capacitor of M_j can be calculated as

$$E_{jmdg} = \frac{4}{3}C_{dgo}\phi\left[\left(1+\frac{V_{jM}}{\phi}\right)^{0.5}(V_{jM}-2\phi)+2\phi\right] + C_{dgo}(V_{lin})^2 \tag{4-13}$$

The subscript j represents the j^{th} MOSFET, while the subscripts d and g represent the drain and gate terminals. A similar designation s applies to the source terminal. The first term represents energy lost as v_{dg} goes from zero to V_{jM}, while the second term represents the

energy lost when v_{dg} goes from $-V_{lin}$ to zero. The drain-gate capacitance is a constant C_{dgo} when $v_{dg} \leq 0$.

Using (4-11), the energy absorbed by the constant gate-source capacitor of M_j is given by

$$E_{jmgs} = C_{gso}[(V_o)^2 + (V_{lin})^2] \tag{4-14}$$

When the gate voltage rises from zero to $V_o + V_{lin}$, the energy lost to the drain-gate and gate-source capacitors is supplied by the gate-drive circuit. When the gate voltage falls to zero from $V_o + V_{lin}$, the energy lost to the drain-gate and gate-source capacitors is donated by the converter power stage. Therefore, in calculating the net energy lost by the power stage of the converter, only one half of the values given in (4-13) and (4-14) are used.

The energy lost to the drain-source capacitor of M_j is given by

$$E_{jmds} = \frac{4}{3} C_{dso}\phi\left[\left(1 + \frac{V_{jM} - V_o}{\phi}\right)^{0.5}(V_{jM} - V_o - 2\phi) + 2\phi\right] \tag{4-15}$$

The values for C_{dgo}, C_{gso}, and C_{dso} can be calculated using the capacitances specified in a MOSFET data book: the input capacitance C_{iss}, the output capacitance C_{oss}, and the reverse-transfer capacitance C_{rss}. The relationships between these capacitances, which are usually specified at $V_{ds} = 25$ V and $V_{gs} = 0$ V, are given as

$$C_{iss} = C_{gso} + C_{dgo}\left(1 + \frac{V_{dg}}{\phi}\right)^{-m} \tag{4-16}$$

$$C_{oss} = C_{dso}\left(1 + \frac{V_{ds}}{\phi}\right)^{-m} + C_{dgo}\left(1 + \frac{V_{dg}}{\phi}\right)^{-m} \tag{4-17}$$

$$C_{rss} = C_{dgo}\left(1 + \frac{V_{dg}}{\phi}\right)^{-m} \tag{4-18}$$

For $\phi = 0.75$ and $m = 0.5$, these relationships simplify to

$$C_{dgo} = 5.86 C_{rss} \tag{4-19}$$

$$C_{dso} = 5.86(C_{oss} - C_{rss}) \tag{4-20}$$

$$C_{gso} = C_{iss} - C_{rss} \tag{4-21}$$

4.2.2. Current Source MOSFET Energy Loss

In this analysis it is assumed that M_C is a p-channel MOSFET. Therefore, the source voltage remains constant at V_{in}, the gate voltage goes from V_{in} down to V_{gate} and back, and the drain voltage goes from $[V_{nM} - (n\text{-}1)(\Delta V_C)]$ up to V_{nM} and back. The energy lost to the drain-gate capacitance is then given by

$$E_{cgd} = \frac{4}{3} C_{dgo}\phi\left[\left(1 + \frac{V_{in} - V_{nM}}{\phi}\right)^{0.5}(V_{in} - V_{nM} - 2\phi) + 2\phi\right] + C_{dgo}(V_{in} - V_{gate})^2 \tag{4-22}$$

where

$$V_{gate} = V_{in} + V_T - \frac{I_{on}}{g_m} \quad ; \quad V_T < 0 \tag{4-23}$$

Only one-half of this energy is used in calculating the net power loss by the converter.

The energy lost to the gate-source capacitance is given by

$$E_{csg} = C_{gso}(V_{in} - V_{gate})^2 \tag{4-24}$$

The energy lost to the gate-source capacitance of M_C is not used in calculating the net energy lost by the power stage of the converter because the current that flows is between V_{in} and the gate drive circuit of M_C.

The energy lost to the drain-source capacitance is given by

$$E_{csd} = \frac{4}{3}C_{dso}\phi\left[\left(1+\frac{V_{in}-V_{nM}}{\phi}\right)^{0.5}(V_{in}-V_{nM}-2\phi)+2\phi\right]+C_{dgo}(V_{in}-V_{nM}-(n-1)\Delta V_C)^2 \tag{4-25}$$

As with the drain-gate capacitance, only one-half of this energy is used in calculating the net power loss by the converter.

4.2.3. Diode Energy Loss

The power diode circuit model [27] consists of a contact resistance in series with a diode having a junction capacitance. As previously stated, this junction capacitance is modeled using (4-8). In the circuit of Fig. 2-1, it can be seen that there are two types of diodes, charge and discharge. The charge diodes (type "A" diodes) are forward-biased during the charge interval. The discharge diodes (type "B" diodes) are forward-biased during the discharge interval. During the charge interval, the j^{th} B-diode voltage goes from V_F to $-V_{jB}$, where

$$V_{jB} = V_o + (j-1)V_F + (j-2)V_{Cj}[(m+d)T] \tag{4-26}$$

During the discharge interval, the j^{th} A-diode voltage goes from V_F to $-(V_{Cj}[(m+d)T] + V_F)$. Neglecting the contact resistance of the diode and V_F, the energy lost to D_{jA} is then given by

$$E_{jA} = \frac{4}{3}C_{jo}\phi\left[\left(1+\frac{V_{Cj}[(m+d)T]}{\phi}\right)^{0.5}(V_{Cj}[(m+d)T]-2\phi)+2\phi\right] \tag{4-27}$$

Neglecting the contact resistance of the diode, the energy lost to D_{jB} is

$$E_{jB} = \frac{4}{3}C_{jo}\phi\left[\left(1+\frac{V_{jB}}{\phi}\right)^{0.5}(V_{jB}-2\phi)+2\phi\right] \tag{4-28}$$

4.2.4. Switching Power Loss

The total energy lost per switching cycle by the power stage of the SCDDC E_s is the sum of the energy lost from each parasitic capacitor of the switching devices, or

$$E_s = \frac{E_{cdg}}{2} + \frac{E_{cds}}{2} + \sum_{j=2}^{n}\left(\frac{E_{jmdg}}{2} + E_{jmds} + \frac{E_{jmgs}}{2} + E_{jA} + E_{jB}\right) \tag{4-29}$$

The total power lost due to switching is then given by

$$P_s = f_s E_s \tag{4-30}$$

The value for Ψ is obtained from (2-8), or

$$\Psi = \sqrt{\frac{P_o}{P_o + P_s}} \tag{4-31}$$

To obtain the desired output voltage V_o the current through M_C during the charge interval must be increased by the factor $1/\Psi$ or

$$I_{Mc} = \frac{I_{on}}{\Psi} \quad ; \quad mT < t < (m+d)T \tag{4-32}$$

The total power lost due to switching by each MOSFET and diode can also be calculated as

$$P_{smc} = (E_{cdg} + E_{cds} + E_{cgs})f_s \tag{4-33}$$

$$P_{jsm} = (E_{jmdg} + E_{jmds} + E_{jmgs})f_s \tag{4-34}$$

$$P_{jsA} = E_{jA}f_s \tag{4-35}$$

$$P_{jsB} = E_{jB}f_s \tag{4-36}$$

Upon examination of (4-12)-(4-36) it should be obvious that for a given circuit the switching power loss is the same value in each of D_{2A}-D_{nA}, while variable in D_{2B}-$D_{nB}$and the switching MOSFETs M_2-M_n. From (4-12) and (4-26) it can be seen that the magnitude of the charge interval voltages across D_{nB} and M_n are greater than D_{jB} and M_j ($j < n$).

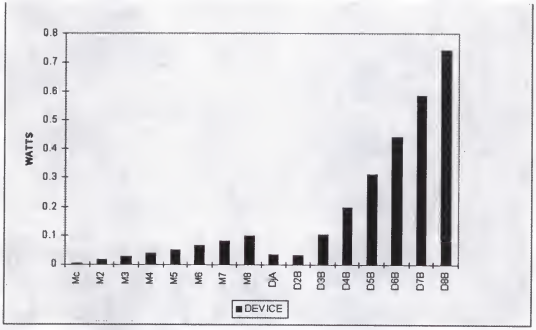


Figure 4-2. Switching power loss in each component for a converter with n =8, V_{in} = 100 V, V_o = 10 V, P_o = 10 W, C = 1.9μF, k = 5, f_s = 207 KHz, ΔV_o = 1%.

Therefore, the greatest switching loss in D_{nB} and M_n is greater than for D_{jB} and M_j ($j < n$). Conversely, the switching loss in D_{2B} and M_2 is less any D_{jB} and M_j where ($j > 2$). Figure 4-2 shows the typical switching loss of each component (as modeled in Chapter 6) for the eight-stage converter of Fig. 4-1.

4.3. Total Power Loss

Using the results of the previous two sections, the total power per device can be calculated by summing the conduction and switching power losses, or

$$P_{tmc} = P_{cmc} + P_{smc} \tag{4-37}$$

$$P_{jtA} = P_{cA} + P_{jsA} \tag{4-38}$$

$$P_{jtB} = P_{cB} + P_{jsB} \tag{4-39}$$

$$P_{jtm} = P_{cm} + P_{jsm} \tag{4-40}$$

$$P_{tC} = P_{cC} \tag{4-41}$$

$$P_{tC1} = P_{cC1} \tag{4-42}$$

4.4. Thermal Analysis

There is a massive amount of literature on the subject of heat transfer, and this dissertation does not intend to present any new material. However, the subject of heat sinking and thermal management must be addressed for a SCDDC, especially for medium output power.

In order to simplify the analysis, several assumptions will be made.

- Heat flows by conduction only (convection and radiation are not discussed).
- The thermal model is static (transient heat flow is ignored).
- The heat dissipated by a component and its heat sink is uniform, i.e. there are no "hot" spots.

The rate at which heat energy is transferred by conduction from a junction at temperature T_j to the air at temperature T_a is defined as Q [23]. It is linearly proportional to the temperature difference between the two interfaces and inversely proportional to the thermal resistance between them, R_θ, or

$$Q = \frac{T_j - T_a}{R_\theta} \tag{4-43}$$

For analysis purposes, it is necessary to define the thermal resistances between three boundaries: the resistance between the junction and the case of the device $R_{\theta jc}$, the resistance between the case and the heat sink $R_{\theta cs}$, and the resistance between the heat sink and the air (ambient) $R_{\theta sa}$. The value for $R_{\theta jc}$ can be found in the MOSFET (or diode) data books. It is a function of the die junction area, the substrate material, attachment method, and package material. The value for $R_{\theta cs}$ is a function of the mounting procedures and can be kept down between 0.1 to 0.2 °C/W if proper procedures are used [3]. The thermal resistance of a heat sink to air of thickness δ (in-cm), cross-sectional area A_θ (in-cm^2), and thermal resistivity ρ_θ is defined as

$$R_{\theta sa} = \frac{\delta \rho_\theta}{A_\theta} \tag{4-44}$$

Because of reliability concerns, it is very important that the junction temperature T_j of the MOSFETs and diodes not exceed the maximum junction temperature rating T_{jmax}. It has been found that a lower junction temperature corresponds to a lower failure rate. For example, a junction operating at temperature of 175°C will have a failure rate three times that of one operating at 125°C.

In a MOSFET, calculating the junction temperature is also important for two other reasons. First, the value for R_{on} is temperature dependent. For example, for a MTM8N40 having a drain current of 6 A, $R_{on} = 0.45\ \Omega$ at 25°C and $R_{on} = 0.80\ \Omega$ at 100°C [36]. Such a large increase in R_{on} can prevent M_C from remaining in saturation during the entire charge interval. Second, T_j determines the maximum power P_{tmax} that can be dissipated by a device. For example, for the MTM8N40 (TO-204 case) the value for P_{tmax} is 150 W at $T_j = 25°C$. However, this value for P_{tmax} must be derated for temperature by the factor $1 / R_{\theta jc} = 1.2$ W/°C for temperatures above 25°C. This means that for $T_j = 125°C$, $P_{tmax} = 30$ W.

Typical values for P_{tmax} and $R_{\theta jc}$ are shown in Table 4-1.

Table 4-1: Typical Maximum Power and Thermal Resistance Values

P_{tmax} (watts)	$R_{\theta jc}$ (°C / watt)
50	2.5
75	1.67
125	1
150	0.83
250	0.5

The junction temperature can be calculated using (4-43) as

$$T_j = T_a + P_t(R_{\theta jc} + R_{\theta cs} + R_{\theta sa}) \tag{4-45}$$

where P_t is the total power dissipated by the device. The size of the heat sink needed can be calculated using (4-44) and (4-45). To find the necessary value for $R_{\theta sa}$, the junction temperature should be set to some value well below T_{jmax}. For a MOSFET, a typical value for T_{jmax} is 150°C for TO-220 and TO-204 packages. Ambient temperature is normally set at 25°C, but may be different depending on environmental conditions. As previously stated, the value for $R_{\theta cs}$ is approximately 0.1 to 0.2 °C/W, and the value for $R_{\theta jc}$ can be found from the device data books. The thermal resistivity for a variety of materials is shown in Table 4-2 [23].

Table 4-2: Thermal Resistivities of Materials Used in Electronic Equipment

Material	Resistivity °C-cm/watt
Still Air	3050
Mylar	635
Silicone Grease	520
Mica	150
Filled silicone grease	130
Alumina	6.0
Silicon	1.2
Beryllia	1.0
Aluminum Nitride	0.64
Aluminum	0.48
Copper	0.25

CHAPTER 5

DYNAMIC ANALYSIS AND COMPENSATION

Knowledge of the open-loop dynamic response of the converter is needed so that a feedback network can be designed to keep the output voltage constant in the presence of changes in input or output parameters such as the input voltage or the output load. Analyzing the dynamics of the converter is also important in the development of large and small-signal equivalent circuits, whose use greatly reduces the time necessary to simulate the converter circuit in PSPICE.

In this chapter, the open and closed-loop dynamic response of the converter is analyzed using the results of Modified State-Space-Averaging derived in Chapter 3. Section 5.1 derives the open-loop input current to output voltage and duty cycle to output voltage transfer functions by perturbing the averaged state-space equation derived in Chapter 3. The averaged state-space equation is also used to derive the large and small-signal equivalent circuits. From the small-signal circuit, several different impedances are calculated, along with the audio susceptibility function. Section 5.2 closes the loop and discusses a method of compensation to optimize the transient response of the closed-loop converter by manipulation of the phase margin of the loop-gain. Section 5.3 calculates the voltage gain of the closed-loop circuit and discusses the effects of feedback on the input and output impedances and other functions of interest. Section 5-4 gives an example of how to implement a closed-loop converter.

5.1. Open-Loop Response

The open-loop transfer functions are now derived [33]. The input vector to state vector transfer function is derived first, followed by the duty cycle to state vector transfer function.

5.1.1. Current Amplitude Control

Assume that a small variation in the input vector

$$u = U + \hat{u} \tag{5-1}$$

causes a similar variation in the state vector

$$x = X + \hat{x} \tag{5-2}$$

The duty cycle is assumed to remain constant, or $d = D$. Substitution into (3-33) gives

$$\dot{X} + \dot{\hat{x}} = A(X + \hat{x}) + B(U + \hat{u}) \tag{5-3}$$

The dynamic model can be extracted from (5-3), and neglecting second-order terms, is given by

$$\dot{\hat{x}} = A\hat{x} + B\hat{u} \tag{5-4}$$

Using Laplace transforms, the input vector to state vector transfer function can be shown to be

$$\frac{\hat{x}}{\hat{u}} = (sI - A)^{-1}B \tag{5-5}$$

Although (5-5) contains four separate transfer functions, the only one that will be considered is the one that relates the input current to the output voltage. Using (3-54), the input current to output voltage transfer function is given by

$$\frac{\hat{v}_0}{\hat{i}_{on}} = G_c(s) = \frac{\frac{nD\Psi}{kC}(s + \omega_c)}{\left(s + \frac{\omega_c}{\omega_c(n-1+k)CR_L + 1}\right)\left(s + \frac{\omega_c(n-1+k)CR_L + 1}{kCR_L}\right)} \tag{5-6}$$

where

$$\omega_c = (1 - \mu)2\pi f_s \tag{5-7}$$

For medium output power or when $k >> n$, a good approximation to (5-6) is given by

$$G_c(s) \approx \frac{\frac{nD\Psi}{kC}}{\left(s + \frac{1}{kCR_L}\right)} \tag{5-8}$$

Equation (5-8) has a single pole, which means that the overall phase of $G_c(s)$ will never be more than –90 degrees at the crossover frequency, and may be much less negative for

large values of $C_1 = kC$ (medium output power). See Appendix B for a more complete derivation.

5.1.2. Duty Cycle Control

To derive the duty cycle to state vector transfer function it is assumed that a small perturbation occurs

$$d = D + \hat{d} \tag{5-9}$$

while the input vector remains constant. Because matrices A and B are complicated functions of d, there is no way to easily factor out $\hat{d}$. Instead, the A and B matrices are expanded in a Taylor series [41] about the steady-state value of the duty cycle D. This allows A and B to be written in the form:

$$A(d-D) = A(D) + a_1(D)(d-D) + (a_2(D)(d-D)^2 + \ldots) \tag{5-10}$$

$$B(d-D) = B(D) + b_1(D)(d-D) + (b_2(D)(d-D)^2 + \ldots) \tag{5-11}$$

Neglecting all terms higher than first-order, evaluation of (5-10) and (5-11) using (5-9) and substitution of (5-2) and (5-10)-(5-11) into (3-33) gives

$$\dot{X} + \dot{\hat{x}} \approx (A + a_1\hat{d})(X + \hat{x}) + (B + b_1\hat{d})U \tag{5-12}$$

where the first-order coefficient matrices, a_1 and b_1, are

$$a_1 = \begin{bmatrix} \frac{1}{kC}\left[\frac{\mu\sigma(n-1)}{(R_{on}+R_{esr})} + \frac{(1-\alpha)(1-\mu)}{R_L}\right] & \frac{-\mu(n-1)}{kC(R_{on}+R_{esr})} \\ \frac{-1}{C}\left[\frac{\mu\sigma}{(R_{on}+R_{esr})} + \frac{(1-\mu)}{(n-1+k)R_L}\right] & \frac{\mu}{C(R_{on}+R_{esr})} \end{bmatrix} \tag{5-13}$$

$$b_1 = \begin{bmatrix} \frac{\Psi}{kC}\left[n-\mu(n-1) - \frac{\mu DT(n-1)}{\alpha C(R_{on}+R_{esr})}\right] & \frac{\mu(n-1)}{k\alpha C(R_{on}+R_{esr})} \\ \frac{\mu\Psi}{C}\left[1 + \frac{DT}{\alpha C(R_{on}+R_{esr})}\right] & \frac{-\mu}{C(R_{on}+R_{esr})} \end{bmatrix} \tag{5-14}$$

where μ and σ evaluated at $d = D$.

The dynamic model can be extracted from (5-12) and, neglecting second-order terms, is given by

$$\dot{\hat{x}} \approx A\hat{x} + \hat{d}(a_1 X + b_1 U) \tag{5-15}$$

Using Laplace transforms, the duty cycle to state vector transfer function can be shown to be

$$\frac{\hat{x}}{\hat{d}} \approx (sI - A)^{-1}(a_1 X + b_1 U) \tag{5-16}$$

Again, the only transfer function of interest is the one relating the duty cycle to the output voltage. Assuming that (3-54) holds, for medium output power or when $k >> n$ this transfer function can be approximated as

$$\frac{\hat{v}_o}{\hat{d}} = G_d(s) \approx \frac{1}{\left(s + \frac{1}{kCR_L}\right)} \cdot \frac{nI_{on}\Psi}{kC} \tag{5-17}$$

Equation (5-17) is similar to (5-8) in that it is a single-pole function, with the overall phase contribution never more than –90 degrees at the crossover frequency. See Appendix B for a more complete derivation.

5.1.3. Averaged State-Space Large-Signal Circuit Model

The averaged state-space equation ((3-33)) is now used to derive the averaged state-space circuit model [33]. Expansion of the averaged state-space equation gives

$$\frac{dv_{C1}}{dt} = \frac{i_{C1}}{kC} = A_{11}v_{C1} + A_{12}v_{Cj} + B_{11}I_{on} + B_{12}V_F \tag{5-18}$$

$$\frac{dv_{Cj}}{dt} = \frac{i_{Cj}}{C} = A_{21}v_{C1} + A_{22}v_{Cj} + B_{21}I_{on} + B_{22}V_F \tag{5-19}$$

where $A_{11}, A_{12}, A_{21}, A_{22}, B_{11}, B_{12}, B_{21}$, and B_{22} are defined in (3-44) and (3-45). Using (3-54), and solving for the currents i_{C1} and i_{Cj}, (5-18) and (5-19) simplify to

$$i_{C1} \approx -\frac{v_o}{R_L} + d\Psi I_{on}(n - \mu n + \mu) + (v_{Cj} - v_o - V_F)\frac{(1-\mu)(n-1)C}{T} \tag{5-20}$$

$$i_{Cj} \approx \mu d\Psi I_{on} - (v_{Cj} - v_o - V_F)\frac{(1-\mu)C}{T} \tag{5-21}$$

A circuit representation of (5-20) and (5-21) is shown in Fig. 5-1 where

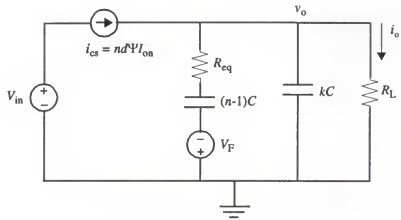


Figure 5-1. State-space averaged circuit model.

$$R_{eq} = \frac{1}{(1-\mu)} \cdot \frac{1}{(n-1)f_s C} \tag{5-22}$$

The circuit in Fig. 5-1 is a large-signal dc circuit model. The steady-state dc output voltage can be calculated directly as

$$V_o = nd\Psi I_{on} R_L \tag{5-23}$$

which is identical to (3-55). The current source in Fig. 5-1 is actually a p-channel power MOSFET, where the channel-length modulation is neglected and the drain current is given using (2-2) as

$$i_{cs} = nd\Psi I_{on} = nd\Psi \cdot K_m(-V_{gs} + V_T) \tag{5-24}$$

Figure 5-2 shows the state-space averaged circuit model with the current source replaced by the large-signal MOSFET model, including the terminal capacitances and drain

resistance [44]. The labels in the MOSFET model of *d*, *g*, and *s* stand for the drain, gate and source, respectively.

5.1.4. Small-Signal Circuit Model

The small-signal circuit model is derived by perturbing the averaged circuit model of Fig. 5-2, which results in the circuit of Fig. 5-3. Neglecting V_F and the second-order terms, the ac resistance term is derived as

$$r_{eq} = \hat{d}\frac{R_{eq}^2}{R_{on} + R_{esr}} \tag{5-25}$$

The perturbed current of the current source is given by

$$\hat{i}_{cs} \approx n\Psi K_m[\hat{d}(-V_{gs} + V_T) - D\hat{v}_{gs}] \tag{5-26}$$

The small-signal circuit model can be found from Fig. 5-3 and is shown in Fig. 5-4. The drain resistance R_D is assumed to be constant, which means that there is no quasi-saturation region in the epidrain [44]. For medium and high voltage MOSFETs with maximum v_{ds} ratings greater than 300 V, $R_D = R_{onp}$. Otherwise, R_D is measured using another method [44].

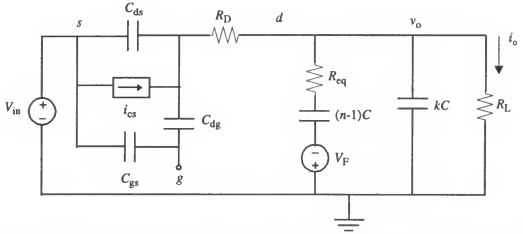


Figure 5-2. State-space averaged circuit model with the MOSFET model in place of the current source.

5.1.5. Impedances and Admittances

The circuit of Fig. 5-4 can be used to derive the open-loop input and output impedances. Using (5-26) and assuming that $d = D$, $\hat{v}_s = \hat{v}_{in}$ and $\hat{v}_g = \hat{v}_d = 0$, the input impedance is given by

$$Z_i(s) = \frac{\hat{v}_{in}}{\hat{i}_s} \approx \frac{s + \dfrac{1}{C_{ds}(R_D + G_c)} \cdot \dfrac{1}{C_x}}{\left(s + \dfrac{nD\Psi g_m}{C_x + g_m C_y (R_{eq} + G_c)}\right)\left(s + \dfrac{C_x + nD\Psi g_m C_y (R_{eq} + G_c)}{C_x C_y (R_{eq} + G_c)}\right)} \tag{5-27}$$

where

$$C_x = C_{gs} + C_{ds} \tag{5-28}$$

$$C_y = C_{ds} + C_{dg} \tag{5-29}$$

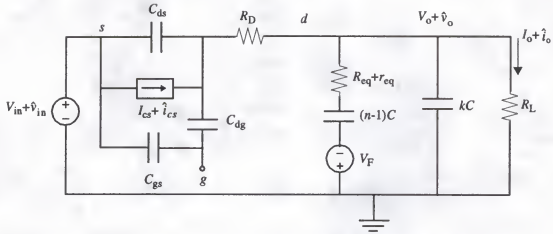


Figure 5-3. Circuit resulting from perturbation of the state-space averaged circuit model.

The poles and zero of (5-27) are at relatively high frequencies as compared to the poles and zero of (5-6) and to the practical values of switching frequencies. Therefore, for the frequencies of interest (which are less than some sub-multiple of the switching frequency), (5-27) can be approximated as

$$Z_1(s) \approx \frac{1}{nD\Psi g_m} \tag{5-30}$$

where the transconductance g_m is given by

$$g_m = K_m = C_o W v_{sat} \tag{5-31}$$

$$g_m = 2K_m = \frac{W}{L} C_o \mu_p (-V_{gs} + V_T) \tag{5-32}$$

for (2-3) and (2-4), respectively.

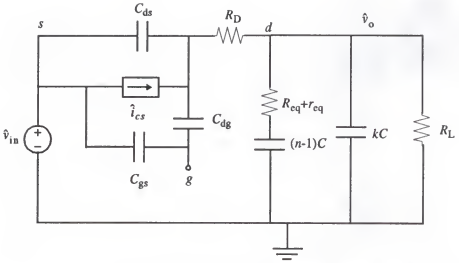


Figure 5-4. Small-signal circuit model for the SCDDC.

Assuming that the impedance looking into the drain of a MOSFET is large at the frequencies of interest, the output impedance is given by

$$Z_o(s) = \frac{\hat{v}_o}{\hat{i}_o} = \frac{s + \dfrac{1}{(n-1)C(R_{eq} + r_{eq})}}{s + \dfrac{1}{kC(R_{eq} + r_{eq})} \cdot \dfrac{1}{1-\alpha}} \cdot \frac{1}{skC} \tag{5-33}$$

Another function of interest is the gate admittance, which relates the gate voltage to the drain current. The gate admittance will be used in the next section to calculate the loop-gain for current-amplitude control. Using the circuit in Fig. 5-4, for a p-channel MOSFET the gate admittance is given by

$$Y_{gate}(s) = \frac{\hat{i}_{cs}}{\hat{v}_g} = \frac{C_{dg}}{(C_{dg} + C_{ds})(R_D + Z_{ps})} \left(\frac{s - \dfrac{nD\Psi g_m}{C_{dg}}}{s + \dfrac{1}{(C_{dg} + C_{ds})(R_D + Z_{ps})}} \right) \tag{5-34}$$

Again, as in (5-27), the pole and zero frequencies of (5-34) are relatively high as compared to the pole of (5-8) and the frequencies of interest. Therefore, (5-34) can be approximated as

$$Y_{\text{gate}}(s) \approx -nD\Psi g_{\text{m}} \tag{5-35}$$

5.1.6. Audio Susceptibility Function

The audio susceptibility function (input voltage to output voltage transfer function) is derived from the input current to output voltage transfer function given by (5-8) and the input impedance given by (5-30). It is assumed that the duty cycle is constant, or $d = D$. The drain and source currents of the current source are assumed to be equal, and are given by

$$\hat{i}_{\text{cs}} = \hat{i}_{\text{d}} = nd\Psi\hat{i}_{\text{on}} \approx \hat{i}_{\text{s}} \tag{5-36}$$

The audio susceptibility function can now be found using (5-8), (5-30) and (5-36) as

$$\frac{\hat{v}_{\text{o}}}{\hat{v}_{\text{in}}} \approx \frac{\dfrac{nD\Psi g_{\text{m}}}{kC}}{\left(s + \dfrac{1}{kCR_{\text{L}}}\right)} \tag{5-37}$$

The dc value of this function is $g_{\text{m}} \cdot R_{\text{L}}$, which means that any low-frequency change in V_{in} can have significant effect on V_{o}.

5.2. Compensation

The output voltage of the converter is to be regulated by controlling the amplitude of or the duty cycle of the current through M_C. This is done by feeding back the output voltage to a compensation and control circuit, forming a closed-loop system, as shown in Fig. 5-5. If the current amplitude is used to regulate the output, the control circuit would supply M_C with a gate voltage that could vary in amplitude while maintaining a constant duty cycle. If the duty cycle is used to regulate the output, the control circuit would supply M_C with a gate voltage that could vary in duty cycle while maintaining a constant amplitude. Because the SCDDC would very often be connected to integrated circuits, the desired output response would have the fastest possible rise time with minimal overshoot, which corresponds to a loop-gain phase margin between 45 and 60 degrees. To obtain the desired transient response, a feedback compensation network $H_c(s)$ found in [50] is used to supply the necessary phase at the crossover frequency.

For current amplitude control, the loop-gain T_{CL} is given by Fig. 5-5(a) as

$$T_{CL} = G_{gate}(s)G_c(s)H_c(s) \tag{5-38}$$

where $G_{gate}(s)$ is given by

$$G_{gate}(s) = Y_{gate}H_{gate} \tag{5-39}$$

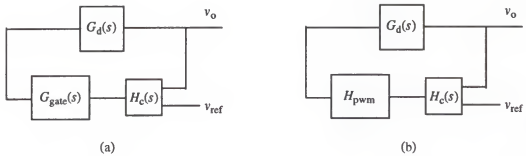


Figure 5-5. Closed-loop system for a SCDDC using current amplitude (a) and duty cycle (b) control.

and H_{gate} is the gain of the gate drive circuit of the current source (in this case it is negative). For duty cycle control T_{CL} is given by Fig. 5-5(b) as

$$T_{CL} = H_{pwm} G_d(s) H_c(s) \tag{5-40}$$

where H_{pwm} is the gain of the Pulse-Width-Modulation circuit. The expression for $H_c(s)$, shown in Fig. 5-6, is given by

$$H_c(s) = \frac{v_c}{v_o} = \frac{-R_f}{R_i} \cdot \frac{C_{f1}}{C_{f1} + C_{f2}} \cdot \frac{1 + \frac{\omega_z}{s}}{1 + \frac{s}{\omega_p}} \approx \frac{-R_f}{R_i} \cdot \frac{1 + \frac{\omega_z}{s}}{1 + \frac{s}{\omega_p}} \qquad C_{f2} << C_{f1} \tag{5-41}$$

where the open-loop gain of the amplifier A_{amp} is neglected and

$$\omega_z = \frac{1}{R_f C_{f1}} \tag{5-42}$$

$$\omega_p = \frac{1}{R_f C_{f2}} \tag{5-43}$$

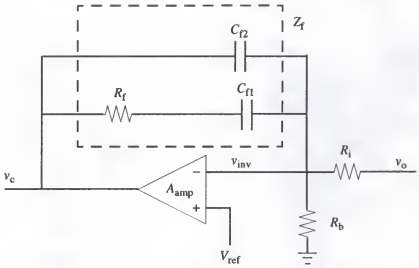


Figure 5-6. Operational amplifier implementation of the compensation network $H_c(s)$.

Figure 5-7 shows the gain and phase characteristics of $H_c(s)$ for an experimental 1 W, four-stage converter.

The frequency response of the closed-loop systems in Fig. 5-5 can be determined by examination of the phase of the loop gain T_{CL} at the crossover frequency ω_{co}, or the frequency where the magnitude of T_{CL} equals one. Without the added phase from the pole and zero of $H_c(s)$, the maximum phase of T_{CL} is only -270 degrees at ω_{co}. This means that although the system is stable, the response of the system is very slow. Therefore, to obtain the desired response the pole and zero of $H_c(s)$ must supply between -30 and -45 degrees of phase at the crossover frequency.

It is assumed that the crossover frequency is to be set to some fraction of the switching frequency, where the fraction is less than one half [39]. It is further assumed that the low-frequency pole of T_{CL} is much less than ω_{co}, or

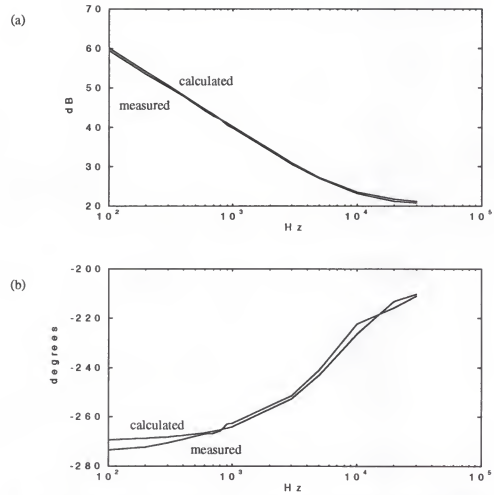


Figure 5-7. The gain (a) and phase (b) for the compensation circuit for a duty cycle controlled SCDDC with P_o = 1 W, V_{in} = 25 *V*, V_o = 5 V, n = 4, k = 19.1, f_s = 100 KHz, C = 0.68 μF, V_{ref} = 2 V, ϕ_m = 60 degrees, R_i = 91 Ω, R_b = 62 Ω, R_f = 1.1 KΩ, C_{f1} = .016 μF, C_{f2} = 1180 pF, P_{Ri} = 0.1 W.

$$\frac{1}{kCR_L} \ll \omega_{co} \tag{5-44}$$

If the following are defined as:

$$\omega_{co} = \sqrt{\omega_z \omega_p} \tag{5-45}$$

$$K = \frac{\omega_{co}}{\omega_z} = \frac{\omega_p}{\omega_{co}} \tag{5-46}$$

then it can be shown that the phase of $H_c(s)$ is given by

$$\angle H_c(s) = -180° - 2\arctan(K^{-1}) = -360° + 2\arctan(K) \tag{5-47}$$

Using (5-47), the phase of T_{CL} is now given by

$$\angle T_{CL} = -90° + \angle H_c(s) = -450° + 2\arctan(K) \tag{5-48}$$

The phase margin ($\phi_m > 0$) is then given by

$$\phi_m = 360° + \angle T_{CL} = -90° + 2\arctan(K) \tag{5-49}$$

The value for K can be found from (5-49), and is given by

$$K = \tan\left(\frac{\phi_m + 90°}{2}\right) \tag{5-50}$$

5.3. Closed-Loop Response

This section looks at the performance of the closed-loop system, especially the output voltage as related to some reference voltage, and the effect of feedback on the output impedance and the input impedances looking into the gate and source of M_C.

5.3.1. Voltage Gain

In the closed-loop system the value of the output voltage of the SCDDC is to be directly related to the value of some reference voltage v_{ref}, or

$$v_o = A_{CL} v_{ref} \tag{5-51}$$

The compensation circuit, shown in Fig. 5-6, can be used to calculate the value of A_{CL} by summing the currents at the inverting terminal of the op-amp, or

$$\frac{v_c - v_{inv}}{Z_f} + \frac{v_o - v_{inv}}{R_i} = \frac{v_{inv}}{R_b} \tag{5-52}$$

where

$$Z_f = \frac{1}{sC_{f2}} \| \left(R_f + \frac{1}{sC_{f1}} \right) \tag{5-53}$$

$$v_{inv} = v_{ref} - \frac{v_c}{A_{amp}} \tag{5-54}$$

and A_{amp} is the open-loop gain of the operational amplifier. A more accurate expression than (5-41) for the gain of the compensation circuit can be shown to be

$$H_c(s) = \frac{v_c}{v_o} = \frac{-Z_f}{R_i} \left(\frac{\frac{-A_{amp} R_i}{R_i + Z_f}}{1 - \frac{A_{amp} R_i}{R_i + Z_f}} \right) \tag{5-55}$$

For a good-quality high-frequency amplifier, A_{amp} is very large for the frequencies of interest [48], and (5-55) can be approximated as

$$H_c(s) = \frac{v_c}{v_o} \approx \frac{-Z_f}{R_i} \tag{5-56}$$

Using (5-52)-(5-56), the equation for A_{CL} can be shown to be

$$A_{CL} = \frac{v_o}{v_{ref}} = \left(1 + \frac{R_i}{R_b} + \frac{R_i}{Z_f}\right) \cdot \varepsilon_A \tag{5-57}$$

$$\varepsilon_A = \frac{T_{CL}}{T_{CL} - 1} - \frac{Z_f}{A_{amp} T_{CL} R_i}\left(\frac{1}{R_i} + \frac{1}{R_b} + \frac{1}{Z_f}\right) \tag{5-58}$$

where T_{CL} is the loop-gain given by (5-38) or (5-40).

The dc ($s = 0$) gain error term ε_{A0} can now be calculated using (5-38)-(5-39), (5-53), (5-56) and (5-58) as

$$\varepsilon_{A0} = 1 \tag{5-59}$$

The percent gain error is then given by

$$\Delta\varepsilon_{A0} = (1 - \varepsilon_{A0}) \cdot 100\% = 0 \tag{5-60}$$

From (5-57)-(5-58), the dc voltage gain is given by

$$A_0 = \left(1 + \frac{R_i}{R_b}\right) \tag{5-61}$$

To find the component values for the compensation circuit, choose some value P_{Ri} as the power dissipation of R_i. Using (5-61), the input component values can be calculated using

$$R_i = \frac{(V_o - V_{ref})^2}{P_{Ri}} \tag{5-62}$$

$$R_b = \frac{R_i}{\left(\frac{V_o}{V_{ref}} - 1\right)} \tag{5-63}$$

Using (5-41)-(5-43) and (5-46) the feedback components can be calculated using

$$R_f = |H_c(\omega_{co})| R_i \tag{5-64}$$

$$C_{f1} = \frac{1}{R_f \omega_z} \tag{5-65}$$

$$C_{f2} = \frac{1}{R_f \omega_p} \tag{5-66}$$

5.3.2. Impedances

Since the output voltage is sampled by the feedback circuit, the output is said to have shunt feedback. Shunt feedback lowers the output impedance, which is now given by [11]

$$Z_{oc} = \frac{(Z_o \parallel R_i)}{1 - T_{CL}} \tag{5-67}$$

Lowering the output impedance is advantageous because the effect of a large increase in output current will have a much smaller effect on the output voltage, as compared to the open-loop circuit. Examination of (5-33) shows that Z_o goes to infinity as the frequency goes to zero, but (5-67) goes to zero at dc.

Since the amplitude of the gate voltage is controlled by the feedback circuit, the input is said to have series feedback. Series feedback increases the input impedance, which is now given by

$$Z_{ic} = Z_i(1 - T_{CL}) \tag{5-68}$$

Increasing the input impedance is advantageous because the effect of a large increase in input voltage will have a much smaller effect on the output voltage, as compared to the open-loop circuit. Examination of (5-27) shows that Z_i is fairly small, which means that even a small variation in input voltage can have a significant effect on the input current, and thus the output voltage. However, (5-68) goes to infinity as the frequency goes to zero which means that even a relatively large variation in input voltage will have a very small effect on the input current and the output voltage.

5.3.3. Audio Susceptibility Function

The closed-loop audio susceptibility function can be calculated using (5-8), (5-37) and (5-68) as

$$\frac{\hat{v}_o}{\hat{v}_{in}} \approx \frac{\dfrac{nD\Psi g_m}{kC}}{\left(s + \dfrac{1}{kCR_L}\right)} \cdot \frac{1}{1 - T_{CL}} \tag{5-69}$$

Again, it is assumed that the duty cycle is constant, or $d = D$. As previously mentioned, the effect of feedback is to reduce the effect of a variation in input voltage on the output voltage. At dc (5-69) goes to zero, which means that even a relatively large variation in input voltage will have a very small effect on the output voltage.

5.4. Design of a Closed-Loop Converter

An example will now be given to illustrate how to design a closed-loop converter. The input parameters are $V_{in} = 24$ V, $V_o = 10$ V, and $P_o = 25$ W. The complete results of the design procedure for this example are presented in Chapter 7.

In this example, a Micro Linear ML4811 High Frequency Power Supply Controller [31] is used as the main component of the feedback loop. The ML4811 uses pulse-width modulation (PWM) to control the output voltage (duty cycle control). Figure 5-8 shows the circuit block-diagram of a two-stage experimental converter with a ML4811 as the control device. Although the ML4811 has many features such as soft start reset, cycle-by-cycle current limit, and under voltage lockout, for simplicity only the input, PWM and output sections are shown.

The switching frequency is chosen to be 100 KHz and the crossover frequency is set to be $f_s/3$. The reference voltage was chosen to be $V_{ref} = 5.1$ V since the ML4811 has

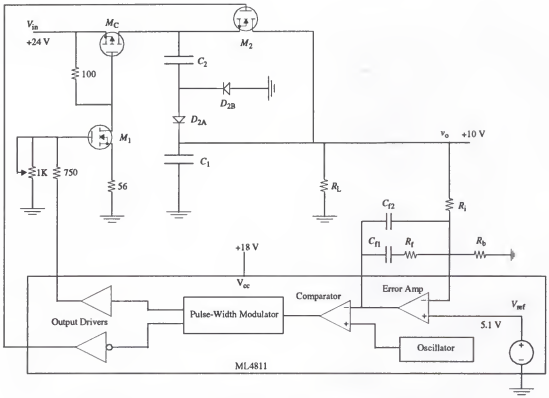


Figure 5-8. Simplified circuit diagram of an experimental 25 W converter.

this voltage as an output on pin 19. An estimate of H_{pwm} can be calculated from the data sheets of the ML4811 by dividing the duty cycle range by the ramp valley to peak voltage. For the ML4811, this value is $H_{pwm} = 0.28$.

If the phase margin is set to 60 degrees, the component values compute to be $R_i = 240\ \Omega$, $R_b = 250\ \Omega$, $R_f = 4\ K\Omega$, $C_{f1} = 4500$ pF, and $C_{f2} = 323$ pF. Figure 5-6 shows the gain and phase plots of the resulting compensation network and Fig. 5-9 shows the gain and phase of the closed-loop gain T_{CL}. It can be seen from Fig. 5-9 that the crossover frequency is approximately 33 KHz, and the phase is approximately –300 degrees at the crossover frequency. This gives a phase margin of 60 degrees.

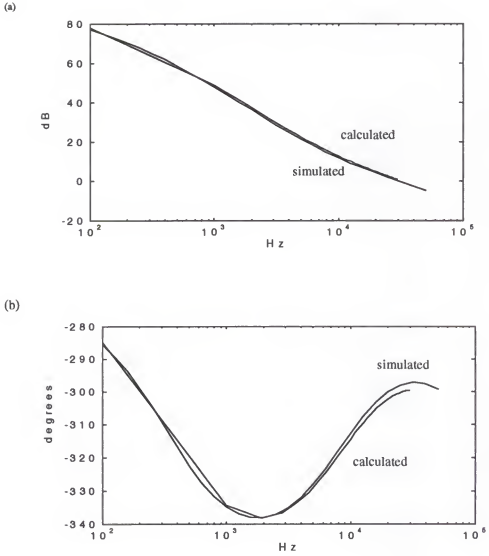


Figure 5-9. The gain (a) and phase (b) of the closed-loop gain T_{CL} for a duty-cycle controlled SCD-DC with P_o = 25 W, V_{in} = 24 *V*, V_o = 10 V, $n = 2$, f_s = 100 KHz, C = 6.8 μF, V_{ref} = 5.1 V, ϕ_m = 60 degrees, R_i = 240 Ω, R_b = 250 Ω, R_f = 4 KΩ, C_{f1} = 4.5 nF, C_{f2} = 323 pF, PSPICE simulation.

CHAPTER 6

DESIGNING A SWITCHED-CAPACITOR DC-DC CONVERTER

As stated in Chapter 1, SCDDCs have been analyzed many times using State-Space-Averaging, and in the previous chapters using Modified State-Space-Averaging. However, there has been little written on how to design a practical SCDDC for a specific application, especially for medium output power.

In designing a SCDDC, there is a trade-off between total capacitance used (which translates into size) and efficiency. For a given application, there are many different solutions that will satisfy the set of input and output specifications, where each different solution may have a different total capacitance. It is the objective of this chapter to present a method of design that will enable the reader to design a SCDDC that has the minimum total capacitance volume for a given input voltage, output voltage, output ripple and minimum efficiency.

This chapter also gives the designer an idea of the component parameters that will be encountered for particular values of input voltage, output voltage and output ripple. The component parameter models are used to calculate such things as R_{on} and the parasitic capacitances that the designer would see in a datasheet. In Chapter 7 these models are used to calculate the limits of converter performance using available components.

Section 6.1 presents the parameter models for the power MOSFETs, power diodes and capacitors. These models give empirical relationships between the parameters needed

in the design procedure and the current and blocking voltage. Section 6.2 discusses the rationale behind how to select the number of stages and the switching frequency, along with the requirements of the gate-drive circuit. Section 6.3 presents the optimized design procedure.

6.1. Component Parameter Models

This section presents the component parameter models empirically derived from manufacturer's data sheets. These models are used in the design procedure in calculating the minimum total capacitance volume for the given converter requirements.

6.1.1. Charging Capacitors

In choosing the type of capacitor to use in a SCDDC, the designer has to take into account such parameters as maximum working voltage, maximum available capacitance, equivalent series inductance (ESL), equivalent series resistance (ESR), size and cost. Based on these criteria, this dissertation recommends using the SupraCap^{TM}, a multi-layer ceramic capacitor made by the AVX Corporation [4]. These capacitors, made especially for use in switching power supplies, feature extremely low ESR and ESL. They can be obtained with working voltages up to 500 V and capacitance values up to 1300 μF. They also come with leadframes for either thru-hole or surface mount assembly.

In using multi-layer ceramic capacitors, the designer must decide which type of dielectric to use, as each one has its own distinct advantage. The C0G (NPO) dielectric has the most stable capacitance with age and frequency. The X7R dielectric has the most stable

capacitance with temperature. The Z5U dielectric provides the highest capacitance for a given size. Since one of the goals of the design procedure is to find the minimum size of the total capacitance, the Z5U dielectric will be used in this dissertation.

In order to compute the volume of the total capacitance, a standard capacitance per unit volume $S(V_{wk})$ as a function of working voltage will be defined. Using the SupraCap™ capacitance data, this relationship is found to be

$$S(V_{wk}) \approx \frac{\left(24000 \frac{\mu F\text{-}V}{in^3}\right)}{V_{wk}} \tag{6-1}$$

where V_{wk} is the capacitor working voltage rating. In the design procedure V_{wk} will be set to the maximum voltage across the capacitor times a safety margin, or

$$V_{wk} \approx S_m V_{Cj}[(m + d)T] \tag{6-2}$$

The maximum value for V_{wk} is 200 V for the Z5U dielectric.

It will also be assumed that R_{esr} and C are inversely proportional to each other. Using the SupraCap™ capacitance curves and specifications, this relationship is found to be

$$R_{esr} \approx \frac{24 m\Omega\text{-}\mu F}{C} \tag{6-3}$$

where C is given in microfarads. A more complete derivation of the capacitor parameter relationships can be found in Appendix C.

6.1.2. MOSFETs

As with the charging capacitance, a standard power MOSFET model for M_2-M_n will be defined using current power MOSFET data books [34][36]. The relationship between blocking voltage V_{block}, average drain current I_{Mj}, and R_{on} for this standard power MOSFET will be given as

$$R_{onmax}(25°C) = 0.1132 \frac{\text{A-}\Omega}{\text{V}^{0.5}} \cdot \frac{\sqrt{V_{block}}}{I_{rating}} \tag{6-4}$$

$$I_{Mj} = \frac{d' \Psi I_{on}}{n-1} \tag{6-5}$$

$$V_{block} = S_m V_{in} \tag{6-6}$$

where $R_{onmax}(25°C)$ is the value of R_{onmax} when the junction temperature is $T_j = 25°C$ and I_{rating} is the minimum current rating of a power MOSFET for a given value of blocking voltage. This value for R_{on} is the maximum allowable value that will fit the data [36]. The minimum allowable value is given as [36]

$$R_{onmin}(25°C) = 5.8(V_{block})^2 + 0.026 \tag{6-7}$$

where the maximum value for V_{block} is 1000 V. The value for I_{rating} as a function of I_{Mj} and V_{block} is given as the maximum of [36]

$$I_{\text{rating}} = \frac{40\ \text{A-V}^{0.5}}{\sqrt{V_{\text{block}}}} \tag{6-8}$$

$$I_{\text{rating}} = I_{\text{Mj}} \tag{6-9}$$

In choosing M_2-M_n from a data book, the designer needs to know the value of $R_{\text{on}}(25°\text{C})$. However, the value of R_{on} used in the design procedure to minimize the total capacitance is the value of R_{on} at the operating junction temperature, or $R_{\text{on}}(T_j)$. This relationship between $R_{\text{on}}(T_j)$ and $R_{\text{on}}(25°\text{C})$ is given by

$$R_{\text{on}}(T_j) = R_{\text{on}}(25°\text{C}) \cdot \left[\frac{0.009}{°\text{C}} \cdot T_j + 0.775\right] \tag{6-10}$$

For reliability reasons, in the design procedure the junction temperature will be set to one half of T_{jmax}, which for most power MOSFETs is $T_{\text{jmax}} = 150°\text{C}$. Using (6-10), the value for $R_{\text{on}}(25°\text{C})$ becomes

$$R_{\text{on}}(25°\text{C}) = \frac{R_{\text{on}}(75°\text{C})}{1.45} \quad ; \quad T_j = 75°\text{C} \tag{6-11}$$

where $R_{\text{on}}(75°\text{C})$ is defined as the value for R_{on} that gives the minimum capacitance volume for a given design.

The zero-bias capacitances of the power MOSFET in picofarads are found from

$$C_{\text{dgo}} = \frac{\frac{0.85\Omega\text{-pF}}{\text{V}} V_{\text{block}} + 81\Omega\text{-pF}}{R_{\text{on}}(25°\text{C})} \tag{6-12}$$

$$C_{dso} = \frac{\frac{1.17\Omega\text{-pF}}{\text{V}} V_{block} + 147\Omega\text{-pF}}{R_{on}(25°\text{C})} \tag{6-13}$$

$$C_{gso} = \frac{\frac{1.1\Omega\text{-pF}}{\text{V}} V_{block} + 33\Omega\text{-pF}}{R_{on}(25°\text{C})} \tag{6-14}$$

In a power MOSFET data book the input, output and reverse transfer capacitances are specified at $V_{ds} = 25$ V and $V_{gs} = 0$ V. These capacitances can be calculated using (4-16)-(4-18).

The relationship between g_m and I_{on} for a p-channel power MOSFET is given by

$$g_m = I_{on} \cdot \frac{0.53 \text{ mhos}}{\text{A}} \quad ; \quad I_{on} \geq 0.94 \text{ A} \tag{6-15}$$

$$g_m = 0.5 \text{ mhos} \quad ; \quad I_{on} < 0.94 \text{ A} \tag{6-16}$$

The threshold voltage is given by $V_T = -3.5$ V, and the value for V_{lin} is set to 10 V.

The maximum value for I_{Mc} is given by

$$I_{Mcmax} = \frac{3000 \text{ A-V}}{V_{block}} \tag{6-17}$$

A more complete derivation of the power MOSFET parameter relationships can be found in Appendix C.

6.1.3. Diodes

Again, as with the charging capacitors and power MOSFETs, a standard diode model will be defined using data from current data books [13][21]. The blocking voltage is assumed to be between 50 and 1000 V, and p-n junction power diodes are used. To increase efficiency, Schottky diodes could be used for blocking voltages less than 100 V, but they will not used in this particular model.

The forward voltage of the diode is given as

$$V_F = k_T[\ln((I_{on}) + \ln(10)(0.0206V_{block} + 7.22))] \tag{6-18}$$

where $k_T = 0.0259$ at $T_j = 25°C$ and $k_T = 0.0302$ at $T_j = 75°C$.

The junction capacitance C_{jo} in picofarads is related to the diode current by

$$C_{jo} = 6528 - 6.28V_{block} \tag{6-19}$$

Finally, the maximum diode current I_{dmax} is given by

$$I_{dmax} = 49.6 - 0.046V_{block} \tag{6-20}$$

A more complete derivation of the power diode parameter relationships can be found in Appendix C.

6.2. Practical Considerations

In this section, advice is given on how to determine the number of stages and the switching frequency for a specific converter. The gate-drive circuit current requirements are also discussed.

6.2.1. Selecting the Number of Stages

The first thing to decide when designing a SCDDC is how many stages to use for a given value for M, where

$$M = \frac{V_{in}}{V_o} \tag{6-21}$$

In previous work [17][52] the number of stages was computed by rounding M down to the nearest integer, which will be defined as n_{max} (if M is an integer value then subtract one to get n_{max}). This gives the maximum possible efficiency, but not necessarily the minimum capacitance volume V_{CT}, given using (6-1) as

$$V_{CT} = \frac{C_T}{S(V_{wk})} \tag{6-22}$$

where C_T is the total capacitance given by

$$C_T = (n - 1 + k)C \tag{6-23}$$

In the design procedure the designer selects a minimum value of efficiency η_{min}. It can be shown that any converter can be designed to use less than n_{max} stages (assuming that $n_{max} > 2$), and that the minimum value for C_T occurs when $n = 2$. However, because of the increase in working voltage as n is reduced the minimum value for V_{CT} does not necessarily occur at $n = 2$. To determine the value for n, the value of η_{max} as given by (3-64) is calculated for $n = 2$ to n_{max}, and these values compared to η_{min}. The minimum value for n, n_{min}, is given where the function $\Delta\eta$ has the smallest positive value, where

$$\Delta\eta = \eta_{max} - \eta_{min} \tag{6-24}$$

The converter is then designed for all integer values of n from n_{min} to n_{max}. The value of n is chosen as that where V_{CT} is minimum.

6.2.2. Selecting the Switching Frequency

Maximizing the switching frequency is important when trying to minimize the size of the converter because, as shown in Chapter 3, the charging capacitance is inversely proportional to switching frequency. It has been reported [14] that a switching frequency of 10 MHz has been used in a 50 W resonant converter. The problem in switching at 10 MHz is that the effects of the packaging parasitics (such as lead inductance) start to become noticeable. The effects of these parasitics have not been modeled in Modified State-Space-Averaging and will not be considered in this dissertation. Therefore, the maximum switching frequency is limited to f_{smax} = 1 MHz.

The value for f_s is determined by the minimum efficiency requirement η_{min}. Using (2-8), (3-63) and (3-64), the value for f_s can be calculated as the minimum of

$$f_s = f_{smax} \tag{6-25}$$

$$f_s = \frac{P_o}{E_s}\left[\left(\frac{nV_o}{V_{in}\eta_{min}}\right)^2 - 1\right] \quad ; \quad f_s < f_{smax} \tag{6-26}$$

6.2.3. Gate-Drive Circuit Requirements

The function of the gate-drive circuit is to supply (or extract) enough charge to (from) the gate of a power MOSFET to switch it from off to on (or vice versa) in a specified amount of time t_s. In Chapter 3 it was assumed that the time it takes for a power MOSFET to switch states is much less than the switching period, or

$$t_s \ll T \tag{6-27}$$

Therefore, in this dissertation it will be assumed that

$$\frac{T}{100} \le t_s \le \frac{T}{50} \tag{6-28}$$

The amount of charge Q_g needed to charge the input capacitance of a power MOSFET gate can be found in the data books in the plot of gate-source voltage V_{gs} vs. gate

charge Q_g. The value for Q_g is taken from the plot where $V_{gs} = V_{lin}$ for M_2-M_n or $V_{gs} = V_{gate}$ for M_C. The current capability of the gate-drive circuit is then calculated from

$$I_{gd} = \frac{Q_g}{t_s} \tag{6-29}$$

6.3. Design Procedure

The design procedure is used to compute the minimum total capacitance volume V_{CT} for the input specifications of input voltage V_{in}, output voltage V_o, output power P_o, minimum efficiency η_{min}, and output ripple ΔV_o. Given these specifications, the design proceeds as follows:

(1) Calculate I_{on} and R_L using

$$R_L = \frac{V_o}{I_{on}} \tag{6-30}$$

$$I_{on} = \frac{P_o}{V_o} \tag{6-31}$$

This initial value of R_L remains constant throughout the design procedure, while I_{on} will be increased by the factor $1/\Psi$ to compensate for the switching power loss.

(2) Calculate n_{max} by rounding down M to the nearest integer, where M is given by (6-21).

$$M = \frac{V_{in}}{V_o} \tag{6-32}$$

If M is an integer then subtract one from M to get n_{max}. Calculate n_{min} using

$$\eta_{min} \approx n_{min} \frac{V_o}{V_{in}} \tag{6-33}$$

If $n_{min} > n_{max}$, then no solution exists for the given input parameters.

(3) Set $n = n_{max}$ and calculate the maximum possible efficiency η_{max} using

$$\eta_{max} = \frac{n V_o}{V_{in}} \cdot 100\% \tag{6-34}$$

Set the duty cycle to $d = 1/n$ for minimum ripple and the blocking voltage to

$$V_{block} = S_m V_{in} \quad ; \quad 1.25 \le S_m \le 2.0 \tag{6-35}$$

(4) Calculate the average currents through M_C and M_j using

$$I_{Mc} = dI_{on} \tag{6-36}$$

$$I_{Mj} = \frac{d' I_{on}}{n-1} \tag{6-37}$$

Calculate the model parameters for M_C (g_m) and M_j ($R_{on}(25°C)$, $R_{onmin}(75°C)$, $R_{onmax}(75°C)$, C_{dgo}, C_{dso}, C_{gso}) using (6-4), (6-7) and (6-11)-(6-15), and setting $R_{on}(25°C) = R_{onmax}(25°C)$

$$g_m = I_{on} \cdot \frac{0.53 \text{ mhos}}{\text{A}} \quad ; \quad I_{on} \geq 0.94 \text{ A} \tag{6-38}$$

$$g_m = 0.5 \text{ mhos} \quad ; \quad I_{on} < 0.94 \text{ A} \tag{6-39}$$

$$R_{onmax}(75°C) = 0.1641 \frac{\text{A-}\Omega}{\text{V}^{0.5}} \cdot \frac{\sqrt{V_{block}}}{I_{rating}} \tag{6-40}$$

$$R_{onmin}(75°C) = 5.8(V_{block})^2 + 0.026 \tag{6-41}$$

$$C_{dgo} = \frac{\frac{0.85\Omega\text{-pF}}{\text{V}} V_{block} + 81\Omega\text{-pF}}{R_{on}(25°C)} \tag{6-42}$$

$$C_{dso} = \frac{\frac{1.17\Omega\text{-pF}}{\text{V}} V_{block} + 147\Omega\text{-pF}}{R_{on}(25°C)} \tag{6-43}$$

$$C_{gso} = \frac{\frac{1.1\Omega\text{-pF}}{\text{V}} V_{block} + 33\Omega\text{-pF}}{R_{on}(25°C)} \tag{6-44}$$

Set V_T = -3.5 V and V_{lin} = 10 V. Calculate the maximum power MOSFET and diode currents, I_{Mcmax} and I_{dmax}, using (6-17) and (6-20)

$$I_{Mcmax} = \frac{3000 \text{ A-V}}{V_{block}} \tag{6-45}$$

$$I_{dmax} = 49.6 - 0.046 V_{block} \tag{6-46}$$

Set I_{max} to the minimum of I_{Mcmax} and I_{dmax}. If I_{Mc} is greater than I_{Mcmax} or if I_{on} is greater than I_{dmax}, then no solution exists for the given input parameters.

(5) Calculate the model parameters for diodes D_{jA} using (6-18) and (6-19)

$$V_F = k_T[\ln((I_{on}) + \ln(10)(0.0206V_{block} + 7.22))] \tag{6-47}$$

$$C_{jo} = 6528 - 6.28V_{block} \tag{6-48}$$

Use these same parameters for D_{jB}.

(6) Set the switching frequency to its maximum limit of $f_s = 1$ MHz. Calculate the switching period as $T = 1/f_s$.

(7) Calculate the maximum allowable value for $V_{Cj}[(m + d)T]$ from

$$V_{Cjmax}[(m + d)T] = \frac{V_{in} - \frac{I_{on}}{g_m} - V_o}{n - 1} - V_F \tag{6-49}$$

Until μ is available from step 8, set $\mu = 0$ and estimate $V_{Cj}(mT)$ using (3-48), as

$$V_{Cj}(mT) = V_o + V_F \quad ; \quad \mu = 0 \tag{6-50}$$

Calculate the minimum value for C using (3-52) and (3-53) as

$$C_{min} = \frac{dTI_{on}}{V_{Cjmax}[(m + d)T] - V_{Cj}(mT)} \tag{6-51}$$

If $C_{min} \leq 0$, decrement n and repeat steps 2-7. If the value of n is already equal to n_{min}, then no solution exists for the given input parameters. Set $k = 1$, $C = C_{min}$

and calculate the value of R_{esr} and R_1 using (6-3) and

$$R_1 = \frac{R_{esr}}{k} \tag{6-52}$$

(8) Calculate μ using (3-28) and (3-40) as

$$\mu = e^{\frac{-d'T}{\tau_{2b}}} \tag{6-53}$$

$$\tau_{2b} = \frac{kC[R_1(R_{on}+R_{esr})+R_L(R_{on}+R_{esr})+(n-1)R_1R_L]}{[R_L(n-1+k)+R_{on}+R_{esr}+kR_1]} \tag{6-54}$$

Calculate the steady-state value of $V_{Cj}(mT)$ and $V_{Cj}[(m+d)T]$ using (3-34)-(3-40) and (3-46).

$$X = -A^{-1}BU \tag{6-55}$$

$$A = \begin{bmatrix} \sigma\theta - \gamma\sigma(n-1)C\left(R_L + \frac{R_{on}+R_{esr}}{n-1}\right) - \frac{1}{\Gamma} & \gamma(n-1)CR_L \\ \gamma\sigma kCR_L & \theta - \gamma kC(R_L+R_1) - \frac{1}{\Gamma} \end{bmatrix} \frac{\Gamma}{T} \tag{6-56}$$

$$B = \begin{bmatrix} \frac{d\Psi}{kC}\left[\theta - \gamma(n-1)C\left(R_L + \frac{R_{on}+R_{esr}}{n-1}\right) + \gamma(n-1)CR_L\right] & \frac{\gamma\Gamma(n-1)CR_L}{T} \\ \frac{d\Gamma\Psi}{C}(\theta - \gamma kC(R_L+R_1) + \gamma CR_L) & \frac{1-\Gamma(\theta-\gamma kC(R_L+R_1))}{T} \end{bmatrix} \tag{6-57}$$

$$\sigma = e^{\frac{-dT}{\tau_1}} \approx 1 - \frac{dT}{kCR_L} \tag{3-58}$$

$$\theta = \tau_{2a} e^{\frac{-(1-d)T}{\tau_{2a}}} - \mu\tau_{2b} \tag{6-59}$$

$$\gamma = e^{\frac{-(1-d)T}{\tau_{2a}}} - \mu \tag{6-60}$$

$$\Gamma = \frac{1}{\tau_{2a} - \tau_{2b}} \tag{6-61}$$

$$\tau_{2a} = C[R_L(n-1+k) + R_{on} + R_{csr} + kR_1] \tag{6-62}$$

$$x_{m+d} = Nx_m + PU \tag{6-63}$$

$$N = \begin{bmatrix} \sigma & 0 \\ 0 & 1 \end{bmatrix} \qquad P = \begin{bmatrix} \frac{dT\Psi}{kC} & 0 \\ \frac{dT\Psi}{C} & 0 \end{bmatrix} \tag{6-64}$$

(9) Using $\phi = 0.75$ V, calculate the switching power loss P_s using (4-12)-(4-30).

$$V_{jM} = V_o + (j-1)V_F + (j-1)V_{Cj}[(m+d)T] \tag{6-65}$$

$$E_{jmdg} = \frac{4}{3}C_{dgo}\phi\left[\left(1 + \frac{V_{jM}}{\phi}\right)^{0.5}(V_{jM} - 2\phi) + 2\phi\right] + C_{dgo}(V_{lin})^2 \tag{6-66}$$

$$E_{jmgs} = C_{gso}[(V_o)^2 + (V_{lin})^2] \tag{6-67}$$

$$E_{\text{jmds}} = \frac{4}{3}C_{\text{dso}}\phi\left[\left(1+\frac{V_{\text{jM}}-V_{\text{o}}}{\phi}\right)^{0.5}(V_{\text{jM}}-V_{\text{o}}-2\phi)+2\phi\right] \tag{6-68}$$

$$E_{\text{cgd}} = \frac{4}{3}C_{\text{dgo}}\phi\left[\left(1+\frac{V_{\text{in}}-V_{\text{nM}}}{\phi}\right)^{0.5}(V_{\text{in}}-V_{\text{nM}}-2\phi)+2\phi\right]+C_{\text{dgo}}(V_{\text{in}}-V_{\text{gate}})^2 \tag{6-69}$$

$$V_{\text{gate}} = V_{\text{in}}+V_{\text{T}}-\frac{I_{\text{on}}}{g_{\text{m}}} \quad ; \quad V_{\text{T}}<0 \tag{6-70}$$

$$E_{\text{csg}} = C_{\text{gso}}(V_{\text{in}}-V_{\text{gate}})^2 \tag{6-71}$$

$$E_{\text{csd}} = \frac{4}{3}C_{\text{dso}}\phi\left[\left(1+\frac{V_{\text{in}}-V_{\text{nM}}}{\phi}\right)^{0.5}(V_{\text{in}}-V_{\text{nM}}-2\phi)+2\phi\right]+C_{\text{dgo}}(V_{\text{in}}-V_{\text{nM}}-(n-1)\Delta V_{\text{C}})^2 \tag{6-72}$$

$$V_{\text{jB}} = V_{\text{o}}+(j-1)V_{\text{F}}+(j-2)V_{\text{Cj}}[(m+d)T] \tag{6-73}$$

$$E_{\text{jA}} = \frac{4}{3}C_{\text{jo}}\phi\left[\left(1+\frac{V_{\text{Cj}}[(m+d)T]}{\phi}\right)^{0.5}(V_{\text{Cj}}[(m+d)T]-2\phi)+2\phi\right] \tag{6-74}$$

$$E_{\text{jB}} = \frac{4}{3}C_{\text{jo}}\phi\left[\left(1+\frac{V_{\text{jB}}}{\phi}\right)^{0.5}(V_{\text{jB}}-2\phi)+2\phi\right] \tag{6-75}$$

$$E_{\text{s}} = \frac{E_{\text{cdg}}}{2}+\frac{E_{\text{cds}}}{2}+\sum_{j=2}^{n}\left(\frac{E_{\text{jmdg}}}{2}+E_{\text{jmds}}+\frac{E_{\text{jmgs}}}{2}+E_{\text{jA}}+E_{\text{jB}}\right) \tag{6-76}$$

$$P_{\text{s}} = f_{\text{s}}E_{\text{s}} \tag{6-77}$$

Calculate Ψ using

$$\Psi = \sqrt{\frac{P_{\text{o}}}{P_{\text{o}}+P_{\text{s}}}} \tag{6-78}$$

Recalculate the value of I_{on} as

$$I_{on} = \sqrt{\frac{P_o}{\Psi^2 R_L}} = \sqrt{\frac{P_o + P_s}{R_L}} \tag{6-79}$$

Calculate the source voltage of M_C as

$$V_{source} = V_o + (n-1)(V_F + V_{Cj}[(m+d)T]) + \frac{I_{on}}{g_m} \tag{6-80}$$

If $V_{source} > V_{in}$ decrement R_{on} and repeat steps 8-9 until $V_{source} \leq V_{in}$. The lower limit of R_{on} is R_{onmin}. If R_{on} reaches R_{onmin} and the condition still exists that $V_{source} > V_{in}$, then no solution exists for the given input parameters.

(10) Compute the output ripple using (A-4)-(A-7) and (A-9).

$$\Delta V_o = v_{C1}^*[(m+d)T + t_{max}] - v_{C1}^*(mT) \tag{6-81}$$

$$v_{C1}^*[(m+d)T + t_{max}] = [\Gamma_1 V_{C1}((m+d)T) + \Gamma_2 V_{Cj}((m+d)T)]e^{\frac{-t_{max}}{\tau_{2a}}} +$$

$$[\Gamma_2 V_{C1}((m+d)T) - \Gamma_2 V_{Cj}((m+d)T)]e^{\frac{-t_{max}}{\tau_{2b}}} \tag{6-82}$$

$$\Gamma_1 \approx \frac{kR_L - R_{on} - R_{esr}}{(n-1+k)R_L - R_{on} - R_{esr}} \tag{6-83}$$

$$\Gamma_2 \approx \frac{(n-1)R_L}{(n-1+k)R_L - R_{on} - R_{esr}} \tag{6-84}$$

$$t_{max} = \tau_{2b} \ln\left[-\frac{\tau_{2a}}{\tau_{2b}} \cdot \frac{\Gamma_2 V_{C1}((m+d)T) - \Gamma_2 V_{Cj}((m+d)T)}{\Gamma_1 V_{C1}((m+d)T) + \Gamma_2 V_{Cj}((m+d)T)}\right] \tag{6-85}$$

If the calculated output ripple is not less than or equal to the desired output ripple, increment C and recalculate R_{esr} and V_{work}. Set R_{on} back to R_{onmax} and repeat steps 8-10.

(11) Calculate the efficiency using (3-63) as

$$\eta = \frac{nV_o}{V_{in}}\Psi \cdot 100\% \tag{6-86}$$

If η is not greater than or equal to the minimum efficiency, reduce the switching frequency and repeat steps 4-11 until the efficiency reaches the desired value.

(12) Calculate the total capacitance and the total capacitance volume using (6-1), (6-22) and (6-23).

$$C_T = (n - 1 + k)C \tag{6-87}$$

$$V_{CT} = C_T \cdot S(V_{wk}) \tag{6-88}$$

$$S(V_{wk}) \approx \frac{\left(24000 \frac{\mu F\text{-}V}{in^3}\right)}{V_{wk}} \tag{6-89}$$

Decrement n and repeat steps 2-12, continuing to decrement n as long as V_{CT} continues to decrease or until n reaches n_{min}.

(13) Increment k and repeat steps 2-13. Continue to increment k until the minimum value for V_{CT} has been reached, which will usually be at $k = 1$, 2 or 3.

(14) To calculate the component values for the compensation circuit, first select the value for the phase margin ϕ_m and the value of the crossover frequency. Note that ϕ_m should be in the range of 45 to 60 degrees and the crossover frequency ω_{co} is less than half of the switching frequency (a nominal value would be one third). Using (5-46) and (5-50), calculate the values of ω_p and ω_z as

$$\tan\left(\frac{\phi_m + 90°}{2}\right) = \frac{\omega_{co}}{\omega_z} = \frac{\omega_p}{\omega_{co}} \tag{6-90}$$

Setting the magnitude of T_{CL} equal to one at the crossover frequency, use (5-8), (5-35), and (5-38)-(5-39) for current amplitude control, or

$$\left|H_c(\omega_{co})\right| = \frac{kC\sqrt{(\omega_{co})^2 + \left(\frac{1}{kCR_L}\right)^2}}{\Psi g_m H_{gate}} \tag{6-91}$$

For duty cycle control use (5-17) and (5-40) to calculate the necessary magnitude of $H_c(\omega_{co})$, or

$$\left|H_c(\omega_{co})\right| = \frac{kC\sqrt{(\omega_{co})^2 + \left(\frac{1}{kCR_L}\right)^2}}{nI_{on}\Psi H_{pwm}} \tag{6-92}$$

Finally, the component values can be found using (5-62)-(5-66), or

$$R_i = \frac{(V_o - V_{ref})^2}{P_{Ri}} \tag{6-93}$$

$$R_b = \frac{R_i}{\left(\frac{V_o}{V_{ref}} - 1\right)} \tag{6-94}$$

$$R_f = |H_c(\omega_{co})| R_i \tag{6-95}$$

$$C_{f1} = \frac{1}{R_f \omega_z} \tag{6-96}$$

$$C_{f2} = \frac{1}{R_f \omega_p} \tag{6-97}$$

Make sure that $C_{f2} << C_{f1}$ as stated in (5-41). A computer program written in Turbo C++ [5] has been written to implement the design procedure, and the source code listing along with a flowchart are given in Appendix D.

CHAPTER 7

CONVERTER PERFORMANCE

In this chapter, the performance of the SCDDC is analyzed in graphical form using the component models and the design procedure of Chapter 6. As with any system, the SCDDC has limits to its performance. Section 7.1 plots the minimum input voltage, the maximum efficiency and the maximum output power for a given output voltage. Section 7.2 plots the total capacitance, the total capacitance volume and the efficiency of the SCDDC as a function of the appropriate input design parameters.

7.1. Performance Limits

In this section the performance limits of the SCDDC are plotted as a function of the output voltage.

7.1.1. Minimum Input Voltage

The first thing a designer might be concerned about is the minimum input voltage necessary for a given output voltage, regardless of the efficiency or the total capacitance. With C very large so that the voltage across the charging capacitors changes very little during the charge interval, and remembering that M_C must be in saturation at all times, this minimum input voltage V_{inmin} can be found from (2-1) and (6-15)-(6-16) as

$$V_{\text{inmin}} \approx \frac{I_{\text{on}}}{g_{\text{m}}} + V_{\text{o}} + (n-1)(V_{\text{F}} + V_{\text{Cj}}(mT)) \tag{7-1}$$

This relationship is shown in Fig. 7-1(a). Since $V_{\text{Cj}}(mT)$ varies with output power, V_{inmin} must also vary with output power. However, the difference in V_{inmin} as P_{o} increases is very small, as shown in Fig. 7-1(b) for $P_{\text{o}} = 1$ W and 100 W, $n = 5$. The difference in the two plots becomes smaller as n and/or P_{o} decreases.

7.1.2. Maximum Output Voltage

As stated in Chapter 6, the maximum working voltage of the capacitors is limited to 200 V. Assuming that the safety margin S_{m} is to be no less than 1.25 and no more than 2.0, this gives the maximum output voltage as $100\text{ V} \le V_{\text{omax}} \le 160$ V. The relationship between V_{omax} and S_{m} is given by

$$V_{\text{omax}} = \frac{200\text{V}}{S_{\text{m}}} \quad ; \quad 1.25 \le S_{\text{m}} \le 2.0 \tag{7-1}$$

7.1.3. Maximum Efficiency

Maximum possible efficiency occurs when $n = n_{\text{max}}$, $V_{\text{in}} = V_{\text{inmin}}$ and $\Psi \approx 1$. As previously stated, C must be very large for V_{in} to be at V_{inmin}. For $\Psi \approx 1$, the switching frequency must be fairly low, which is possible because C is very large. Under these conditions, η_{max} is given using (3-64) and (7-1) as

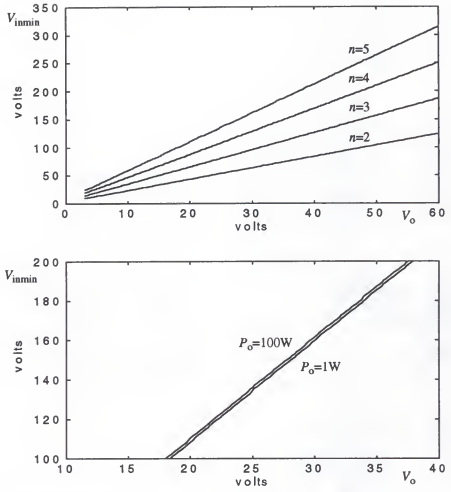


Figure 7-1. Minimum input voltage as a function of output voltage for different values of n, P_o = 100 W (a) and for n = 5, P_o = 100 Wand P_o = 1 W (b).

$$\eta_{max} \approx \frac{n_{max} V_o}{\frac{I_{on}}{g_m} + V_o + (n-1)(V_F + V_{Cj}(mT))} \tag{7-2}$$

This relationship is shown in Fig. 7-2 for different values of n and P_o. It can be seen that the maximum efficiency increases as output voltage increases, flattening out as the output voltage goes above 10 V. As the output voltage decreases below 10 V, the maximum

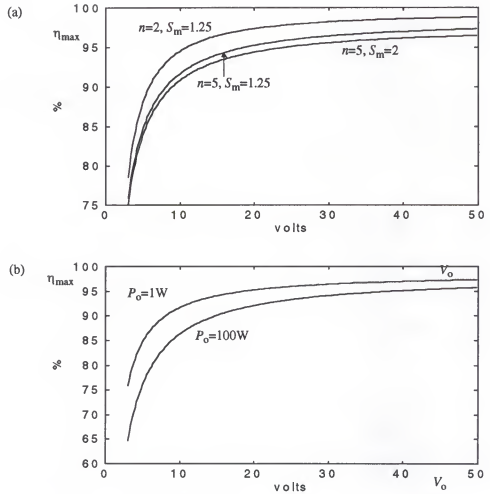


Figure 7-2. Maximum efficiency as a function of output voltage for $n = 2$ and $n = 5$ for $P_o = 1$ W (a), and for $n = 5$, $S_m = 1.25$, $P_o = 1$ W and $P_o = 100$ W (b).

efficiency begins to decrease very rapidly. It can be seen that the SCDDC is not very efficient for small values of output voltage where $V_o \approx (n-1)V_F$, but can be very efficient for larger values of output voltage where $V_o \gg (n-1)V_F$.

7.1.4. Maximum Output Power

Assuming that $V_{in} \geq V_{inmin}$ and that C is large enough to meet the ripple and output power specifications, the maximum output power for a given value of M is determined by the maximum MOSFET and diode currents, I_{Mjmax} and I_{dmax}. The maximum value of the two currents, defined as I_{max}, is shown as a function of V_{block} in Fig. 7-3. The maximum output power is then given by

$$P_{omax} = V_o I_{max} = \frac{V_{in}}{M} I_{max} \tag{7-3}$$

which is shown in Fig. 7-4 as a function of V_o. It can be seen from the figure that the MOSFET current given in (6-17) dominates I_{max}.

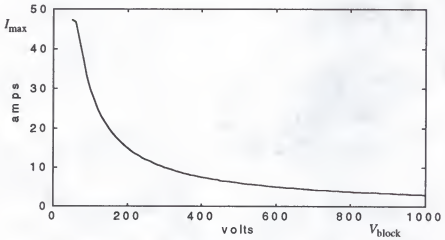


Figure 7-3. Maximum charging current as a function of blocking voltage.

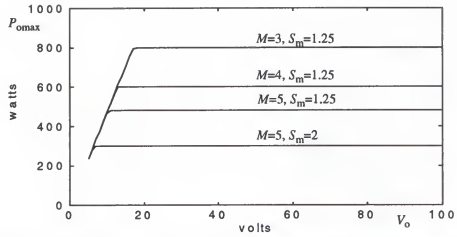


Figure 7-4. Maximum output power as a function of output voltage for different values of M and S_m.

7.2. Performance Parameters

In this section the minimum total capacitance used and the minimum total capacitance volume of the SCDDC are plotted as functions of the input design parameters.

7.2.1. Total Capacitance

The total capacitance C_T used by a converter is a function of the input design parameters. The first parameter to be considered is the output power which, as shown in Figure. 7-6, has a direct relationship to C_T. In Fig. 7-5(a) C_T is plotted as a function of P_o for $V_o = 10V$ and different values of M. In Fig. 7-5(b) C_T is plotted as a function of P_o for $M = 5$ and different values of V_o. In both plots $n = n_{max}$, $\Delta V_o = 0.1\%$, $k = 2$, and $\Delta\eta = 5\%$.

The next parameter of interest is the minimum efficiency η_{min}. It was shown in (3-63) that efficiency is a function of n, so it would be of interest to plot C_T vs. n. As stated

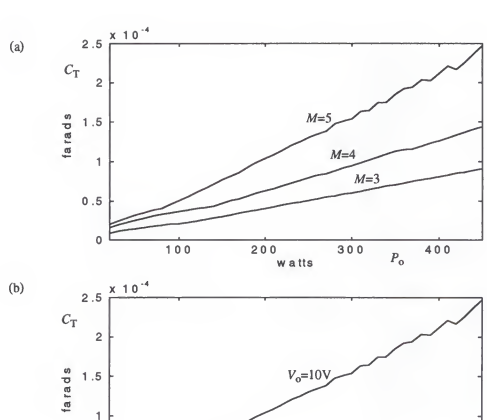


Figure 7-5. Total capacitance as a function of output power for V_o = 10V and different values of M (a), and for M = 5, and different values of V_o, (b). In both cases ΔV_o = 0.1%, $n = n_{max}$, k = 2, S_m = 1.25, and $\Delta\eta$ = 5%.

in Chapter 6, any converter can be built with $n = 2$ stages, and this is where C_T is at its minimum value of C_{Tmin}. Figure 7-6(a) shows the value of C_T as a function of n for different values of P_o for a converter with V_o = 10 V, M = 7, k = 2, and ΔV_o = 0.1%. In this case the converter can be built using n = 2, 3, 4, 5, or 6 stages, depending on the value of P_o and the value of η_{min}. The plot shows that C_T does not necessarily decrease as P_o decreases, especially as P_o becomes less than 10 W. The reason for this is that the switching

frequency must decrease to meet the efficiency specification, which increases C_T. Figure 7-6(b) shows the value of f_s for the corresponding values of n in Fig. 7-7(a) for $P_o = 1$ W. For $P_o = 10$ W and $P_o = 100$ W the switching frequency is $f_s = 1$MHz for each value of n.

The minimum efficiency was also shown to be a function of the switching frequency in (6-25)-(6-26). The switching frequency has an inverse relationship to C_T, and this relationship is shown in Fig. 7-7.

The next parameter of interest is the output ripple. As would be expected, the total capacitance has an inverse relationship to the output ripple. In Fig. 7-8, C_T is plotted as a function of ΔV_o for $P_o = 100$ W, $V_o = 10$ V, $M = 5$, $n = 4$, $k = 2$, and $\Delta\eta = 5\%$.

Although the value of k is not an input parameter, it does have a relationship to C_T. An example showing how C_T varies with k is given in Fig. 7-9. It can be seen that the output ripple affects the value of k where C_T is minimum. In these cases, the minimum value for C_T occurs at $k = 2$, $k = 2$ or 3, and $k = 3$ for $\Delta V_o = 0.1\%$, $\Delta V_o = 0.5\%$, and $\Delta V_o = 1\%$, respectively. It turns out that C_T is always minimum when $k = 2$ or 3.

7.2.2. Total Capacitance Volume

As with the total capacitance, the total capacitance volume V_{CT} is dependent on the input parameters. However, because V_{CT} also depends on the capacitor working voltage V_{work}, it is not necessarily minimum where C_T is minimum. The capacitor working voltage

will stay fairly close to V_o for small values of k, but will increase significantly for much larger values of k, as shown in Fig. 7-10.

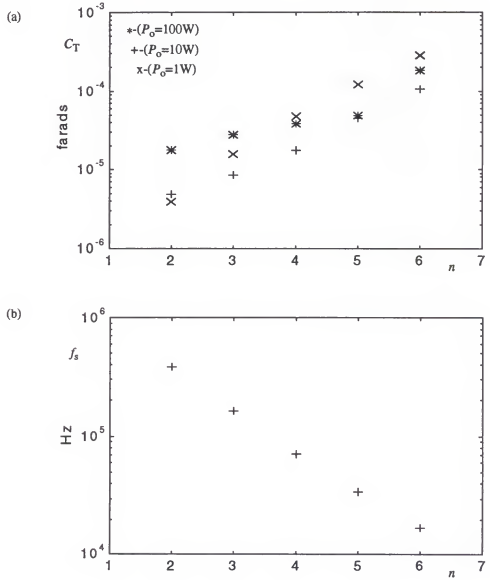


Figure 7-6. Total capacitance as a function of n for different values of P_o (a), and switching frequency as a function of n for $P_o = 1$ W (b), for $V_o = 10$ V, $M = 7$, $k = 2$, $\Delta V_o = 0.1\%$, $S_m = 1.25$, and $\Delta\eta = 5\%$.

It was stated earlier that $C_T = C_{Tmin}$ when $n = 2$ and $k = 2$ or 3. If the value of k is much larger than two V_{CT} may be minimum at a larger value of n, while C_T is still minimum for that value of k at $n = 2$. Figure 7-11(a) shows an example of the variation of V_{CT} as a function of n for $k = 2$, while Fig. 7-11(b) shows another example of V_{CT} as it varies with n when $k = 100$. In the design procedure the value of k will always be set to the value where V_{CT} is a minimum, which is either $k = 2$ or 3. Therefore, for small k the total capacitance volume can be approximated as

$$V_{CT} \approx \frac{C_T(V_o + V_F)}{24000 \frac{\mu F\text{-}V}{in^3}} \tag{7-4}$$

Since V_{CT} is a function of the same parameters as C_T, the plots showing these relationships will be given without further discussion. Figure 7-12 shows the value of V_{CT}

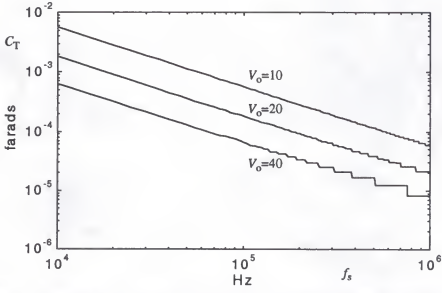


Figure 7-7. Total capacitance as a function of switching frequency for different values of V_o, for $P_o = 100$ W, $M = 5$, $k = 2$, $n = n_{max}$, $\Delta V_o = 0.1\%$, $S_m = 1.25$, and $\Delta\eta = 5\%$.

as a function of P_o for different values of V_o and M for a converter with $k = 2$, $\Delta\eta = 5\%$, and $\Delta V_o = 0.1\%$. The switching frequency has an inverse relationship to V_{CT}, and this relationship is shown in Fig. 7-13. In Fig. 7-15, V_{CT} is plotted as a function of ΔV_o for $P_o = 100$ W, $V_o = 10$ V, $M = 5$, $n = 4$, $k = 2$, and $\Delta\eta = 5\%$.

7.2.3. Efficiency

The relationship of efficiency as a function of output load is an important one for dc-dc converters. Figure 7-15 shows this relationship for a converter with $V_o = 10$ V, $M = 5$, $n = 4$, $k = 2$, $\Delta V_o = 0.1\%$, $S_m = 1.25$, and $\Delta\eta = 5\%$ for different values of P_o.

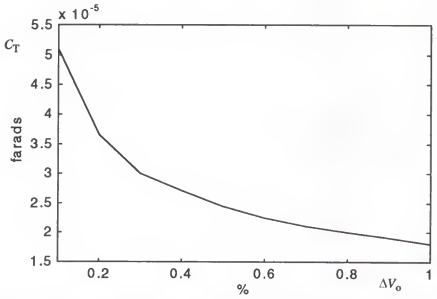


Figure 7-8. Total capacitance as a function of output ripple for $P_o = 100$ W, $V_o = 10$ V, $M = 5$, $k = 2$, $n = n_{max}$, and $\Delta\eta = 5\%$.

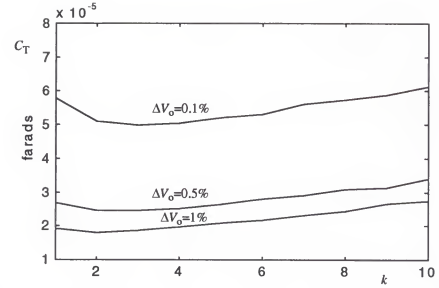


Figure 7-9. Total capacitance as a function of k for P_o = 100W, M = 5, and V_o = 10V for different values of ΔV_o.

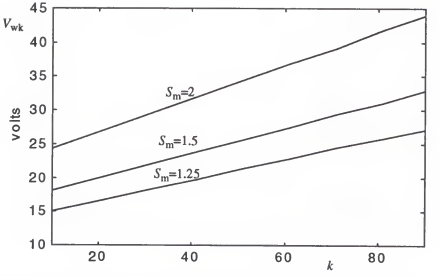


Figure 7-10. Capacitor working voltage as a function of k for P_o = 1 W, V_o = 10 V, M = 5, n = 2, and ΔV_o = 1%.

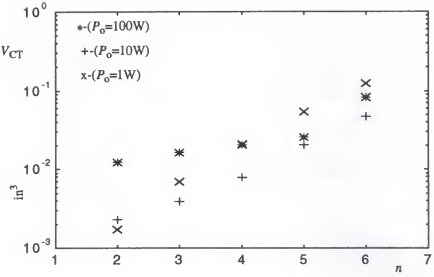


Figure 7-11. The total capacitance volume as a function of n for different values of P_o for $V_o = 10\text{V}$, $P_o = 10\text{W}$, $M = 7$, $k = 2$, $\Delta V_o = 0.1\%$, and $S_m = 1.25$.

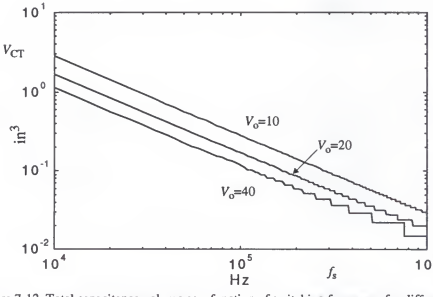


Figure 7-12. Total capacitance volume as a function of switching frequency for different values of V_o, for $P_o = 100\text{ W}$, $M = 5$, $k = 2$, $n = n_{max}$, $\Delta V_o = 0.1\%$, $S_m = 1.25$, and $\Delta\eta = 5\%$.

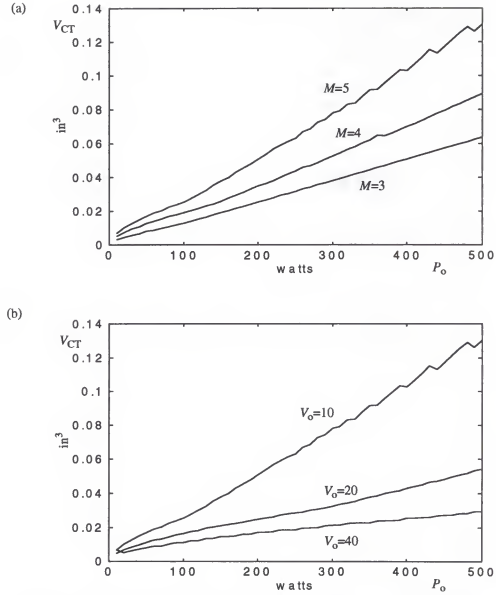


Figure 7-13. Total capacitance volume as a function of output power for $V_o = 10$V and different values of M (a), and for $M = 5$ and different values of V_o, (b). In both cases $\Delta V_o = 0.1\%$, $n = n_{max}$, $k = 2$, $S_m = 1.25$, and $\Delta\eta = 5\%$.

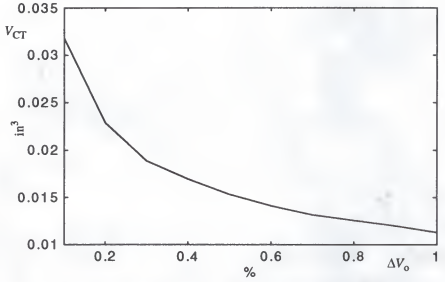


Figure 7-14. Total capacitance volume as a function of output ripple for $P_o = 100$ W, $V_o = 10$ V, $M = 5$, $k = 2$, $n = n_{max}$, $S_m = 1.25$, and $\Delta\eta = 5\%$.

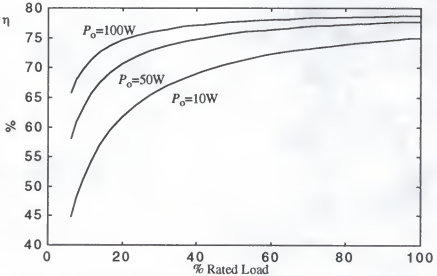


Figure 7-15. Efficiency as a function of rated output load for different values of P_o for a converter with $V_o = 10$ V, $M = 5$, $k = 2$, $n = 4$, $\Delta V_o = 0.1\%$, $S_m = 1.25$, and $\Delta\eta = 5\%$.

CHAPTER 8

VERIFICATION OF ANALYSIS RESULTS

In this chapter, the analysis results of the preceding chapters are verified using simulation and experimental data. In Section 8.1 the dc analysis presented in Chapter 3 is verified by using a design example. An experimental circuit similar to the design example is fabricated to show that a high-efficiency, medium-power converter is feasible. Experimental data is shown to closely agree with analysis and simulation results. Section 8.2 verifies the switching loss analysis presented in Chapter 4. A table showing the calculated and simulated values of output voltage at 100 KHz and 1 MHz is given. Section 8.3 verifies the dynamic analysis given in Chapter 5. An experimental converter is built using a printed-circuit card, and the open-loop transfer functions are measured. The converter is then operated closed-loop and the voltage gain, audio susceptibility function and impedances are measured.

8.1. Verification of the DC Analysis

In this section the dc analysis of Chapter 3 is verified using a 48 W prototype converter. The prototype will show that a high-efficiency medium-power converter is feasible, and simulation and experimental data will be used to verify the analysis results. The specifications for the SCDDC are shown in Table 8-1. Because of limitations in obtaining the necessary parts for an optimum design, certain restrictions were placed on the

component parameters. These were: MTP8P10 for M_C, 1N5822 for D_{jA} and D_{jB}, and

Table 8-1: Input specifications for the 48 W prototype.

Parameter	Value
V_{in}	55 V
V_o	12 V
P_o	48 W
ΔV_o	0.8 %

MTP10N10E for M_j, while the switching frequency was set at f_s = 100 KHz. The component parameters are shown in Table 8-2. Because the largest available capacitor was 10 μF, the value of k had to be chosen so that the ripple specification could be met. Using the design procedure in Chapter 6, the results shown in Table 8-3 were obtained. Since the circuit was operated open-loop, the closed-loop parameters in step 14 were not calculated.

Table 8-2: Component parameters for the 48 W prototype.

Parameter	Value
g_m	2 mhos
V_F	0.3 V
C_{jo}	1.032 nF
$R_{on}(25°C)$	0.25 Ω
C_{iss}	600 pF
C_{oss}	400 pF
C_{rss}	100 pF
R_{esr}	2.5 mΩ

Table 8-3: Circuit parameters for the 48 W prototype.

Parameter	Value
f_s	100 KHz
I_{on}	4.007 A
n	4
d	0.25
Ψ	0.9982
C	9.7 μF
k	9

The PSPICE file used for the simulation is shown in Fig. 8-1. An experimental prototype similar to this example was built and tested using perforated fiberglass board. Since it was difficult to obtain small multi-layer ceramic (MLC) capacitors, relatively large polyester film capacitors were used. The footprint of the power circuit measured 114 mm x 152 mm (4.5 inches x 6 inches), and the height was about 25.4 mm (1 inch). The large circuit layout introduced large parasitic inductances and resistances, causing oscillations and switching spikes which can be seen in the ripple waveform of Fig. 8-2(a).

The results of the PSPICE simulation and the experimental prototype are shown in Table 8-4. The difference in efficiency of the prototype and the simulation (4.8%) is due to the power consumption of the prototype gate-drive circuit.

The drain voltage of M_C is shown in Fig. 8-2(b), and the current through M_4 is shown in Fig. 8-2(c). The shapes of the waveforms obtained from the prototype are very similar to their PSPICE counterparts shown in Figs. 1-2 and 2-3.

Table 8-4: Comparision of calculated, simulated and experimental results for the 48 W prototype.

	Calculated	Simulated	Experimental
Output Voltage	12.0 V	12.0 V	12.0 V
Output Ripple	0.8 %	0.78 %	0.83 %
Efficiency	87.1 %	87.1 %	82.3 %
$V_{Cj}[(m+d)T]$	13.18 V	13.4 V	13.4 V

8.2. Verification of the Switching Loss Analysis

To verify the switching loss analysis found in Chapter 4, several circuits with different output voltages and number of stages were simulated. To provide an equal comparison, the output power was kept at a constant 1 W and the MOSFETs and diodes used were always the IRF520 and 1N5819, respectively. In a real design the IRF520 and 1N5819 might not be used at such a low power level, but they were used in this case to make the effect of the switching losses easier to see. In each simulation the charging current I_{on} was increased to compensate for the effect of the switching losses as discussed in the design procedure given in Chapter 6.

Because PSPICE models the drain-gate capacitance as a constant value independent of bias [51], the MOSFET model in PSPICE had to be modified to include a voltage-

```
55VDC TO 12VDC, n=4, 100KHz, d=.25, k=9, 48 watt, C=9.7uf, Ion=4.007 A, Ron=.3
*variable drain-gate capacitor
Ion 0 1 PULSE(0 4.007 0 50ns 50ns 2.45us 10us)
VMC 14 0 PULSE(0 1 0 50ns 50ns 2.45us 10us)
VM 15 0 PULSE(0 22 2.55us 50ns 50ns 7.35us 10us)
R4 2 3 .0025
R3 5 6 .0025
R2 8 9 .0025
R1 11 12 .00028
RL 11 0 3
D4A 4 5 d1n5822
D4B 0 4 d1n5822
D3A 7 8 d1n5822
D3B 0 7 d1n5822
D2A 10 11 d1n5822
D2B 0 10 d1n5822
C4 3 4 9.7uf IC=12.3
C3 6 7 9.7uf IC=12.3
C2 9 10 9.7uf IC=12.3
C1 12 0 87.3uf IC=11.97
SMC 1 2 14 0 SMOD
X4 2 15 11 mosfet
X3 5 15 11 mosfet
X2 8 15 11 mosfet
.subckt mosfet 1 2 3
Mx 1 2 3 3 IRF520
Cx 1 4 100pf
Ex 4 2 poly(1) 1 4 1 0 0 0 0 .00001
.ends
.model SMOD vswitch(ron=.5)
.model IRF520 NMOS(Level=1 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0 Vmax=0 Xj=0
+Tox=100n Uo=600 Phi=.6 Rs=.1459 Kp=20.79u W=.73 L=2u Vto=3.59
+Rd=80.23m Rds=444.4K Cbd=622.1p Pb=.8 Mj=.5 Fc=.5 Cgso=517.9p
+Cgdo=0 Rg=6.675 Is=2.438p N=1 Tt=137n)
.model D1N5822 D(Is=8.425u Rs=34.63m Ikf=2.37 N=1 Xti=0 Eg=1.11 Cjo=1.032n
+M=.6736 Vj=.75 Fc=.5 Isr=9.599u Nr=2)
.option RELTOL=.005
.tran .1us 600us 0 100ns UIC
.probe
.end
```

Figure 8-1. PSPICE file used to verify the design example in Section 7.1.

dependent drain-gate capacitance. The drain-gate capacitance of the MOSFET used in the simulation was modeled as [16]

$$C_{dg} = \frac{C_{dgo}}{1 + ap(v_{dg})^{p-1}} \tag{8-1}$$

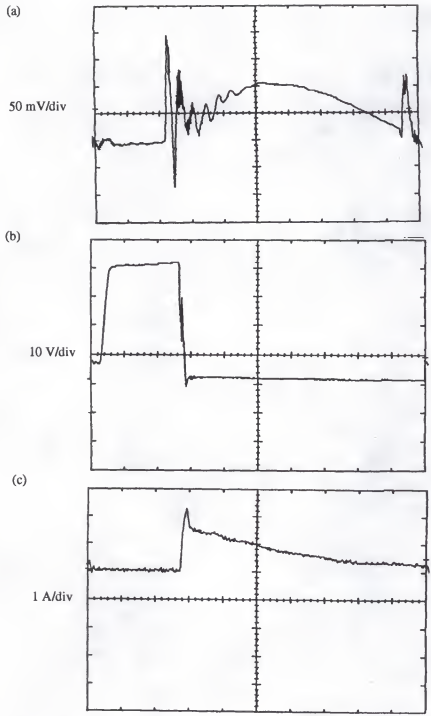


Figure 8-2. Output ripple (a), drain voltage of M_C (b), and current through M_4 (c), from an experimental converter with P_o = 48 W, V_{in} = 55 *V*, V_o = 12 V, n = 4, I_{on} = 4 A, R_L = 3 Ω, C = 10 μF, k = 9, f_s = 100 KHz. Horizontal scale is 1 μs/div.

where, for the IRF520, $a = 10^{-5}$ and $p = 5$. As long as the drain-gate voltage is positive, the model gives a fairly good approximation to the drain-gate capacitance [43].

Table 8-1 shows the calculated and simulated output voltages for 1 W converters switched at 100 KHz and 1 MHz. At 100 KHz (and below) the calculated and simulated values match up very well, especially for low n and/or low output voltage. At 1 MHz the calculated and simulated values begin to show greater variance, especially as n and/or the output voltage increases. It was expected that as n increased, the difference between calculated and simulated values would increase. Any error in calculating the switching loss of one device would be multiplied by the number of devices, and the more devices that are in the circuit the greater the error. The frequency dependence can be explained by the fact that the energy loss is fairly constant regardless of the switching frequency, but the power loss is directly proportional to the switching frequency. As the power loss increases, its effect on the output voltage becomes more pronounced. For example, if $E_{loss} = 0.2$ μjoules/ cycle, then at $f_s = 100$ KHz, $P_{loss} = 0.02$ W and at $f_s = 1$ MHz, $P_{loss} = 0.2$ W. If the desired output power is 1 W, then $P_o = 0.98$ W at $f_s = 100$ KHz and $P_o = 0.8$ W at $f_s = 1$ MHz. From (4-31), any error in calculating P_{loss} obviously introduces a greater error in calculating the output voltage at a switching frequency of 1 MHz than at 100 KHz.

Table 8-5: Output voltages for 1 W converters switched at 100 KHz and 1 MHz, PSPICE simulation.

Number of stages n	Calculated Output Voltage V_o	Simulated Output Voltage V_o @f_s = 100 KHz	Simulated Output Voltage V_o @f_s = 1 MHz
3	10 V	9.95 V	9.77 V
4	5 V	5.02 V	5.04 V
4	12 V	11.72 V	10.40 V
4	15 V	14.55 V	12.20 V
8	5 V	4.85 V	3.85 V

8.3. Verification of the Dynamic Analysis

In this section the dynamic analysis of Chapter 5 is verified using simulation and experimental data from two 25 W prototype converters. The first converter was not optimally designed, since it had to be constructed using available parts. This converter was used to verify the open-loop characteristics. The second converter was more optimally designed, but still had a few restrictions because of the available parts. It was used to verify the closed-loop characteristics.

8.3.1. Converter Design

The design specifications for the first 25 W converter given in Table 8-6. The same restrictions apply to this example as for the 48 W converter, and the component and circuit parameters are given in Tables 8-7 and 8-8, respectively. These restrictions were: MTP8P10 for M_C, NSQ03A04 for D_{jA} and D_{jB}, MTP10N10E for M_j, and the switching

frequency was set at f_s = 100 KHz. The value of k was set to 16.2 because of the available parts.

The design specifications for the second converter, shown in Fig. 8-3, are the same as in Table 8-6 except that the output ripple is now changed to 0.65 %. The same restrictions apply to this example as in the first, with the component parameters given in Table 8-7. The only difference is R_{csr}, which is now equal to 0.4 mΩ. This converter was more optimally designed for minimum capacitance, and the value of k was set to 1.0. The output voltage was to be regulated by controlling the duty cycle, and the design procedure in Chapter 6 gave the results shown in Table 8-9.

Table 8-6: Input specifications for the first 25 W prototype.

Parameter	Value
V_{in}	24 V
V_o	10 V
P_o	25 W
ΔV_o	0.32 %

Table 8-7: Component parameters for the first 25 W prototype.

Parameter	Value
g_m	2 mhos
V_F	0.4 V
C_{jo}	1.0 nF
$R_{on}(25°C)$	0.25 Ω
C_{iss}	600 pF
C_{oss}	400 pF
C_{rss}	100 pF
R_{esr}	1.2 mΩ

Table 8-8: Circuit parameters for the first 25 W prototype.

Parameter	Value
f_s	100 KHz
I_{on}	2.501 A
n	2
d	0.5
Ψ	0.9995
C	6.8 μF
k	16.2

Table 8-9: Circuit parameters for the second 25 W prototype.

Parameter	Value
f_s	100 KHz
I_{on}	2.501 A
n	2
d	0.5
Ψ	0.9995
C	20 μF
k	1.0
ϕ_m	60 degrees
V_{ref}	5.1 V
R_i	240 Ω
R_b	250 Ω
R_f	728 Ω
C_{f1}	24.4 nF
C_{f2}	1.8 nF

The two 25 W experimental prototypes were built using a small, multi-layer printed circuit card. The prototypes used surface-mounted multi-layer ceramic capacitors and diodes to reduce the effects of parasitic resistances and inductances. The footprints of the circuits measured only 76.2 mm x 63.5 mm (3 inches x 2.5 inches), and the height was about 12.7 mm (0.5 inch). The converter was operated closed-loop using a Micro Linear ML4811 High Frequency Power Supply Controller, as discussed in Chapter 5 and shown again in Fig. 8-4.

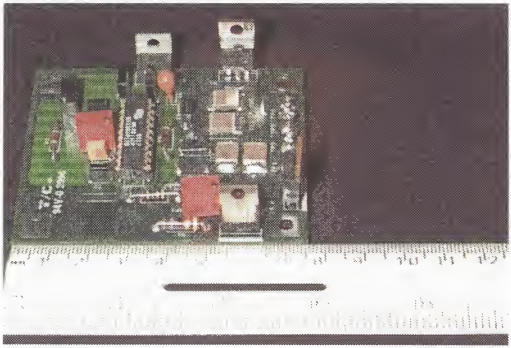


Figure 8-3. Photograph of the second 25 W converter.

8.3.2. Dynamic Measurement Setup Configuration

The open and closed-loop transfer functions were measured using the two 25 W prototypes and a Hewlett-Packard 3577B Network Analyzer [19]. The first prototype was operated open-loop by disconnecting R_1 from the output, while the second was operated closed-loop.

Referring to Fig. 8-4, the output voltage to input current transfer function was measured by injecting the output signal of the HP 3577B onto the base of M_1 through a 10 KΩ resistor and a 150 μF capacitor, modulating the gate-source voltage of M_C. The current through M_C was then measured using a Tektronix P6021 current probe [47], which

was fed into the reference input of the HP 3577B. The output voltage of the prototype was fed directly into channel A of the network analyzer.

The output voltage to duty cycle transfer function was measured by injecting the output signal of the HP 3577B onto the noninverting input pin of the ML4811 through a 10 KΩ resistor and a 150 μF capacitor. The DC level of the noninverting pin was set to 5.1 V using a resistive divider with a series 1 KΩ resistor and a 1 KΩ resistor to ground. The reference input of the analyzer was also connected to its output, which meant that the attenuation network of the 10 KΩ resistor and the 1 KΩ resistor had to be factored out of the result. The output voltage of the prototype was fed directly into the channel A input of the network analyzer.

The input impedance was measured by injecting the output signal of the HP 3577B onto the base of M_1 through a 10 KΩ resistor and a 150 μF capacitor, modulating the gate-source voltage of M_C. The reference input of the analyzer was also connected to its output, which meant that the attenuation network of the 10 KΩ resistor and the 1 KΩ potentiometer had to be factored out of the result. The current through M_C was then measured using a Tektronix P6021 current probe, which was fed into the channel A input of the HP 3577B.

The output impedance was measured by injecting the output signal of the HP 3577B onto C_1 through a 10 Ω resistor and a 150 μF capacitor. The reference input of the analyzer was also connected to its output. The output voltage of the prototype was fed directly into the channel A input of the network analyzer. The load resistor's contribution to the output impedance had to be factored out of the final result.

The audio susceptibility function was measured by injecting the output signal of the HP 3577B onto the base of M_1 through a 10 KΩ resistor and a 150 μF capacitor, modulating the gate-source voltage of M_C. The reference input of the analyzer was also connected to its output, which meant that the attenuation network of the 10 KΩ resistor and the 1 KΩ resistor had to be factored out of the result. The output voltage of the prototype was fed directly into the channel A input of the network analyzer.

8.3.3. Open-Loop Response

As was stated earlier, the open-loop transfer functions were measured using the first prototype, and simulated using the small-signal equivalent circuit of Fig. 5-4.

Figure 8-5(a) shows a PSPICE simulation of the open-loop transient responses of the large-signal equivalent circuit and the actual switching circuit. Figure 8-5(b) uses the large-signal equivalent circuit to show the transient responses of the closed-loop system. In Fig. 8-5(b) the reference voltage is ramped up to its steady-state value and the closed-loop output voltages for both the switching and equivalent circuits are plotted. It can be seen that both the open and closed-loop responses of the two circuits are exact matches.

The output voltage to input transfer functions were measured and plotted versus the calculated values in Figs. 8-6 and 8-7. Figure 8-6 shows the output voltage to input current transfer function (gain and phase), while Fig. 8-7 shows the output voltage to duty cycle transfer function. Good agreement between calculated and measured values can be seen. PSPICE simulations of these transfer functions using the equivalent circuit of Fig. 5-1 were also found to agree very well with the calculated values.

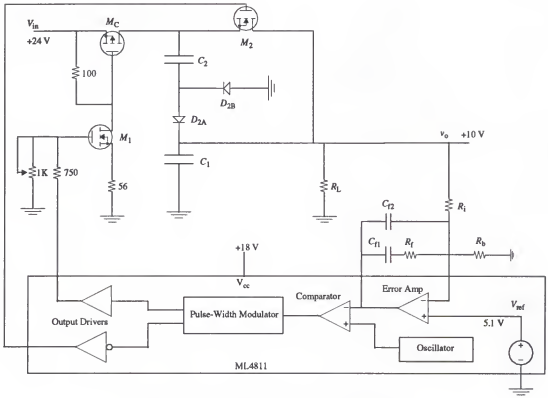


Figure 8-4. Circuit diagram for the 25 W prototypes.

The gain and phase of the open-loop audio susceptibility function was measured and plotted versus its calculated values in Fig. 8-8. As predicted by (5-37), the dc value is $(g_m \cdot R_L)$ with a break frequency of $1/kCR_L$. Good agreement between calculated and measured values can be seen. PSPICE simulations of this transfer function using the

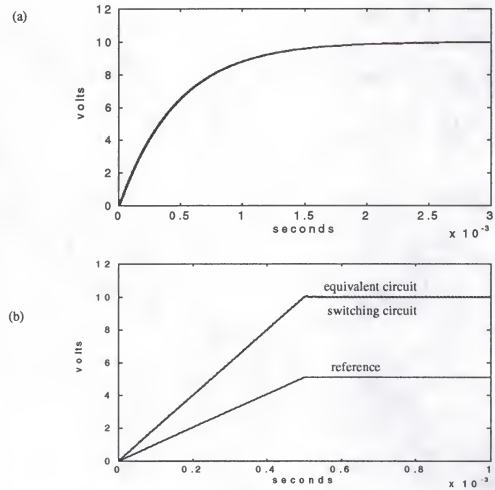


Figure 8-5. Open-loop (a) and closed-loop (b) equivalent and switching circuit transient responses of the closed-loop output voltages for the first and second prototypes where $V_{ref} = 5.1$ V, $\phi_m = 60$ degrees, $R_i = 240\ \Omega$, $R_b = 250\ \Omega$, $R_f = 4$ KΩ, $C_{f1} = 4.5$ nF, $C_{f2} = 325$ pF, PSPICE simulation.

equivalent circuit were also found to agree very well with the calculated values. The open-loop input and output impedances were measured and plotted versus their calculated values in Figs. 8-9 and 8-10. Good agreement between measured and calculated values was observed. PSPICE simulations of these impedances using the equivalent circuit were also found to agree very well with the calculated values.

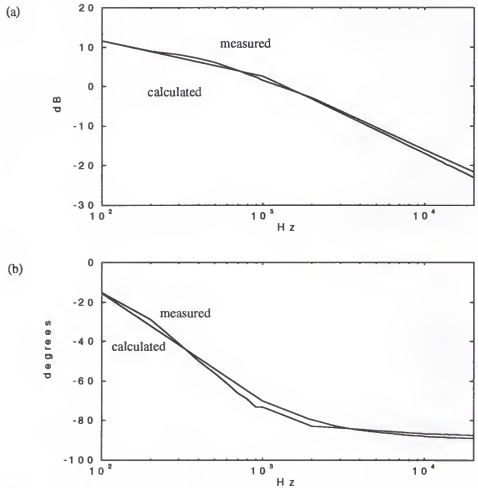


Figure 8-6. Magnitude (a) and phase (b) of the open-loop output voltage to input current transfer function for the first prototype converter with P_o = 25 W, V_{in} = 24 *V*, V_o = 10 V, n = 2, f_s = 100 KHz, I_{on} = 2.5 A, g_m = 2 mhos, R_L = 4 Ω, C = 6.8 μF, R_{esr} = 3.5 mΩ, k = 16.2, R_{on} 25°C = 0.25 Ω, V_F = 0.4 V.

8.3.4. Closed-Loop Response

The second prototype was used to measure the closed-loop transfer functions. The dc gain equation of (5-61) was verified using the prototype converters and by PSPICE simulation. The gain and phase of the closed-loop audio susceptibility function is plotted in Fig. 8-11. As predicted by (5-69), the magnitude of the closed-loop function is reduced

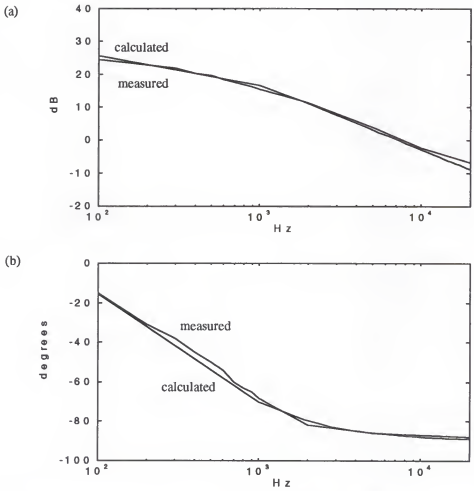


Figure 8-7. Magnitude (a) and phase (b) of the open-loop output voltage to duty cycle transfer function for the first prototype converter.

by the loop-gain. Good agreement between calculated and measured values can be seen. PSPICE simulations of this transfer function using the equivalent circuit were also found to agree very well with the calculated values.

The closed-loop input and output impedances were measured and plotted versus their calculated values in Figs. 8-12 and 8-13. Good agreement between measured and calculated values was observed. PSPICE simulations of these transfer functions using the

equivalent circuit were also found to agree very well with the calculated values. As predicted, the input impedance is increased by the loop-gain, while the output impedance is decreased by it.

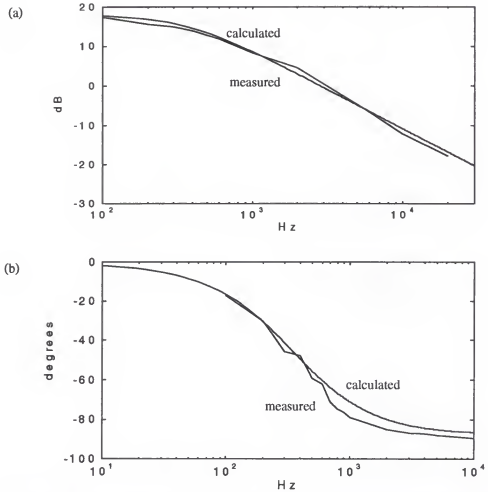


Figure 8-8. Gain (a) and phase (b) of the open-loop audio susceptibility function for the first prototype converter.

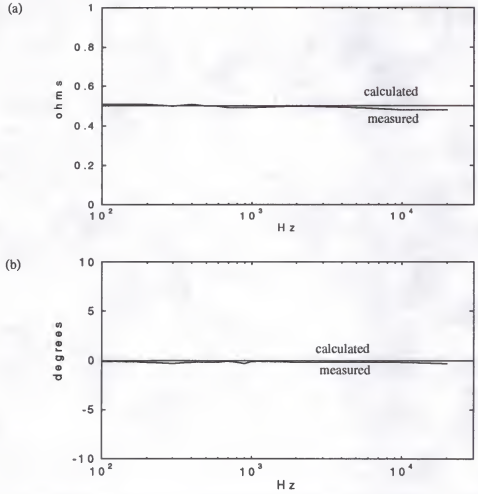


Figure 8-9. Gain (a) and phase (b) of the open-loop input impedance for the first prototype converter.

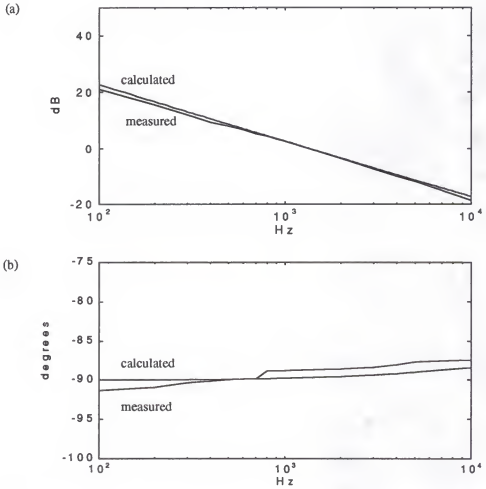


Figure 8-10. Gain (a) and phase (b) of the open-loop output impedance for the first prototype converter.

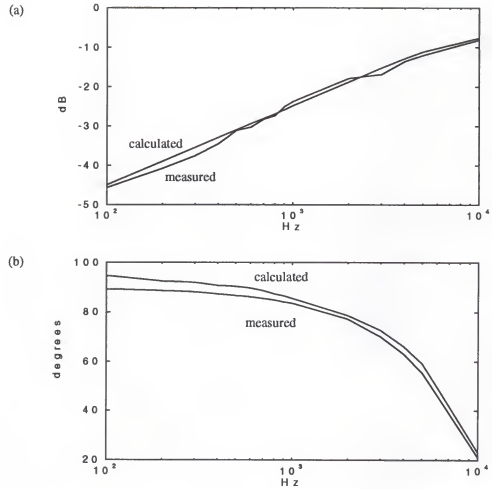


Figure 8-11. Gain (a) and phase (b) of the closed-loop audio susceptibility function for the second prototype SCDDC where $V_{ref} = 5.1$ V, $\phi_m = 60$ degrees, $R_i = 240\ \Omega$, $R_b = 250\ \Omega$, $R_f = 728\ \Omega$, $C_{f1} = 24.4$ nF, $C_{f2} = 1.8$ nF.

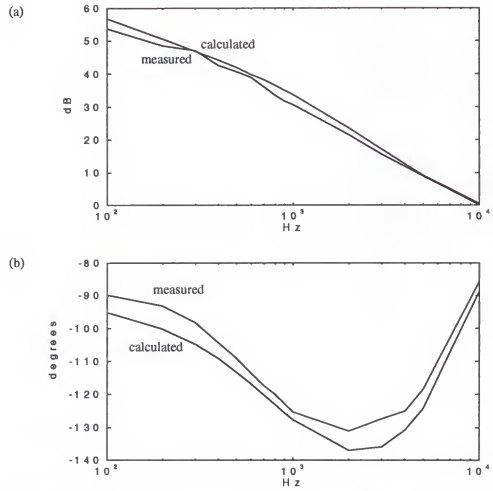


Figure 8-12. Gain (a) and phase (b) of the closed-loop input impedance for the second prototype SCDDC where V_{ref} = 5.1 V, ϕ_m = 60 degrees, R_i = 240 Ω, R_b = 250 Ω, R_f = 728 Ω, C_{f1} = 24.4 nF, C_{f2} = 1.8 nF.

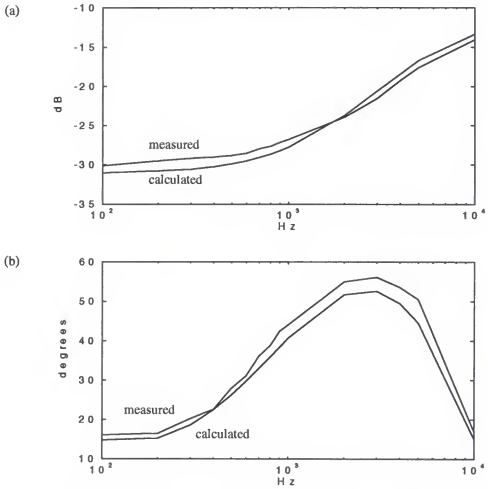


Figure 8-13. Gain (a) and phase (b) of the closed-loop output impedance for the second prototype SCDDC where V_{ref} = 5.1 V, ϕ_m = 60 degrees, R_i = 240 Ω, R_b = 250 Ω, R_f = 728 Ω, C_{f1} = 24.4 nF, C_{f2} = 1.8 nF.

CHAPTER 9

SUMMARY AND CONCLUSIONS

This dissertation has analyzed the various operating characteristics of a representative switched-capacitor dc-dc converter topology. A new technique for analyzing switched-mode converters with nonlinear ripple was introduced. This technique, called Modified State-Space-Averaging, was used to derive the dynamic and steady-state operating conditions for the switched-capacitor dc-dc converter. The effects of switching losses on the output voltage were analyzed by calculating the energy lost in the junction capacitances of the active devices. A design procedure based on analysis results was presented, and was verified using simulation and experimental results.

Chapter 2 introduced the switched-capacitor voltage converter topology that is the focus of this dissertation. The switching operation of the circuit was discussed, along with two methods (input current and duty ratio) for controlling the output voltage. Equivalent circuits for both the charge and discharge intervals were given, along with justification for the inclusion of the switching losses in the state-space equations.

Chapter 3 introduced the analysis problem by giving the background for State-Space-Averaging, and provided the justification for Modified State-Space-Averaging. A numerical example was given to give a comparision between the two. The switched-capacitor dc-dc converter was analyzed using Modified State-Space-Averaging, and practical approximations were made to allow the analysis results to be simplified into a

usable format. These approximations allowed the derivation of the steady-state operating conditions, and calculation of the values of output voltage, output ripple, charging capacitor voltage, and efficiency.

Chapter 4 analyzed the power dissipation (conduction and switching) in the SCDDC and used basic thermal analysis to determine if a device was operating within its maximum ratings.

Chapter 5 used the averaged state-space equation derived from MSSA to obtain the open-loop transfer functions and impedances, along with the large-signal and small-signal equivalent circuits for the converter. These equivalent circuits provided a reduction in the time needed to simulate a converter circuit. This chapter also looked at the effect of the feedback loop on the transfer functions, impedances, and output voltage of the converter. Analysis and modification of the closed-loop gain allowed the designer to set the frequency response of the system. An example was given to show how to implement the feedback loop in a closed-loop converter.

Chapter 6 presented a design procedure based on analysis results derived from Modified State-Space-Averaging. The procedure gave the smallest total capacitance (and size) for the set of input parameters of output voltage, output power, output voltage ripple and efficiency. Standard parameter models of the MOSFETs, diodes, and capacitors used in the proceudure were presented. Performance limits of the SCDDC were also discussed.

Chapter 7 analyzed the performance of the SCDDC in graphical form. In this chapter, the minimum possible input voltage, the maximum possible efficiency, and the

maximum possible output power were all plotted as a function of output voltage. The design procedure in Chapter 6 was then used to obtain curves for the total capacitance used and the total capacitance volume of the SCDDC as a function of the input design parameters.

Chapter 8 presented design examples, and compared analytical, simulation and experimental results. In this chapter, the analysis results of the preceding chapters are verified using simulation and experimental data. Design examples were presented for two medium-power converters. Experimental circuits similar to the design examples were fabricated to show that high efficiency, medium-power converters are feasible. Experimental data was shown to closely agree with analysis and simulation results. Simulation data showing the effect of switching losses on the output voltage at switching frequencies of 100 KHz and 1 MHz was given. Good agreement between calculated and simulated values was shown, except as noted.

There are several areas where further research is needed. First, capacitor technology must develop to the point where the integration of a several hundreds of microfarads capacitor is possible. Until that time, methods for reducing the capacitance needed by a converter must be pursued. It has been found that modification of the switching technique presented in Chapter 2 can lead to a reduction in the output capacitance needed for a particular value of output ripple. One promising technique that has been developed by this author is called sequential switching, where the charging capacitors are discharged into the load one at a time. This technique allows the output capacitance to be reduced by at least

n-1, where n is the number of stages. Although sequential switching has been analyzed in matrix form using Modified State-Space-Averaging, closed-form expressions for the state variables similar to those shown in Chapter 3 have not been derived because of the algebraic complexity. Likewise, dynamic analysis has not been performed for the same reason.

Another way to reduce the capacitance needed is to increase the switching frequency. However, as the frequency is increased above 1 MHz, the model used in this dissertation may have to be modified to include the parasitic inductances of the MOSFET and diodes. This would make obtaining a closed-form solution for the capacitor voltages and output ripple very difficult.

Research is also needed to show how temperature affects the performance parameters of the circuit such as output voltage ripple, capacitor voltage, and efficiency. Since these parameters are significantly affected by component parameters such as R_{on}, R_{esr} and the parasitic capacitances, it would be interesting to know the temperature dependence of the component parameters affects the performance of the circuit.

It is believed that switched-capacitor dc-dc converters will be able to meet the requirements of low to medium power applications. However, more research has to be done before the idea of a fully-integrated SCDDC becomes reality.

APPENDIX A

DERIVATION OF THE OUTPUT RIPPLE EQUATION

The equation for the steady-state output voltage ripple is derived in Chapter 3 from

$$\Delta V_o = \max(v_o^*) - \min(v_o^*) \tag{A-1}$$

There are two cases that must be considered in evaluating (A-1). For $d > 1/n$, (A-1) becomes

$$\Delta V_o = v_o^*[(m+d)T + t_{max}] - v_o^*[(m+d)T] \tag{A-2}$$

where t_{max} is shown in Fig. A-1. For $d \leq 1/n$, (A-1) becomes

$$\Delta V_o = v_o^*[(m+d)T + t_{max}] - v_o^*(mT) \tag{A-3}$$

where t_{max} is shown in Fig. A-2. As explained in Chapter 3, the minimum ripple condition is when $d = 1/n$. For this minimum-ripple condition, the value of ΔV_o is given by (A-3), which can be written using (3-54) as

$$\Delta V_o = v_{C1}^*[(m+d)T + t_{max}] - v_{C1}^*(mT) \tag{A-4}$$

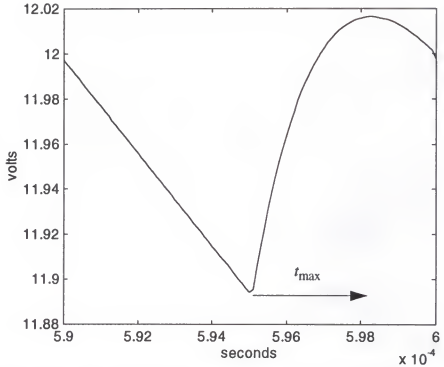


Figure A-1. Output ripple for an SCDDC with P_o = 48 W, V_{in} = 55 *V*, V_o = 12 V, n = 4, d = 0.5, f_s = 100 KHz, I_{on} = 2.002 A, R_L = 3 Ω, C = 9.6 μF, R_{esr} = 0.003 Ω, k = 10, R_{on} = 0.3 Ω, V_F = 0.3 V, PSPICE simulation.

To obtain an expression for (A-4) it is necessary to know $v_{C1}{}^*(t)$ during the discharge interval, and the value of t_{max} can be found from where the derivative of $v_{C1}{}^*(t)$ equals zero. Expansion of (3-16) gives

$$v_{C1}{}^*(t) = [\Gamma_1 V_{C1}((m+d)T) + \Gamma_2 V_{Cj}((m+d)T)]e^{\frac{-[t-(m+d)T]}{\tau_{2a}}} + [\Gamma_2 V_{C1}((m+d)T) - \Gamma_2 V_{Cj}((m+d)T)]e^{\frac{-[t-(m+d)T]}{\tau_{2b}}} \quad \text{(A-5)}$$

where

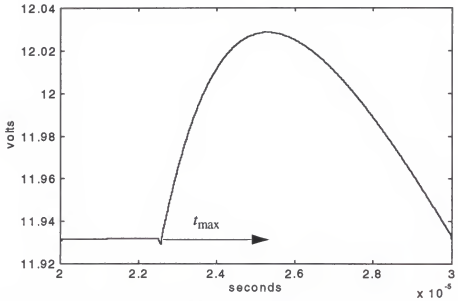


Figure A-2. Output ripple for an SCDDC with $P_o = 48$ W, $V_{in} = 55$ V, $V_o = 12$ V, $n = 4$, $d = 0.25$, $f_s = 100$ KHz, $I_{on} = 4.004$ A, $R_L = 3\ \Omega$, $C = 9.6\ \mu$F, $R_{esr} = 0.003\ \Omega$, $k = 10$, $R_{on} = 0.3\ \Omega$, $V_F = 0.3$ V, PSPICE simulation.

$$\Gamma_1 \approx \frac{kR_L - R_{on} - R_{esr}}{(n-1+k)R_L - R_{on} - R_{esr}} \tag{A-6}$$

$$\Gamma_2 \approx \frac{(n-1)R_L}{(n-1+k)R_L - R_{on} - R_{esr}} \tag{A-7}$$

The derivative of $v_{C1}{}^*(t)$ is then given by

$$\dot{v}_{C1}{}^*(t) = -\frac{1}{\tau_{2a}}[\Gamma_1 V_{C1}((m+d)T) + \Gamma_2 V_{Cj}((m+d)T)]e^{\frac{-[t-(m+d)T]}{\tau_{2a}}} - \frac{1}{\tau_{2b}}[\Gamma_2 V_{C1}((m+d)T) - \Gamma_2 V_{Cj}((m+d)T)]e^{\frac{-[t-(m+d)T]}{\tau_{2b}}} \tag{A-8}$$

Substituting $t = (m + d)T + t_{max}$, the value of t_{max} is found by setting the derivative in (A-8) to zero, or

$$t_{max} = \tau_{2b} \ln\left[-\frac{\tau_{2a}}{\tau_{2b}} \cdot \frac{\Gamma_2 V_{C1}((m+d)T) - \Gamma_2 V_{Cj}((m+d)T)}{\Gamma_1 V_{C1}((m+d)T) + \Gamma_2 V_{Cj}((m+d)T)}\right] = \tau_{2b} \ln \Phi^{-1} \qquad \text{(A-9)}$$

It can be seen from (A-9) that

$$\Phi = e^{\frac{-t_{max}}{\tau_{2b}}} \qquad \text{(A-10)}$$

The expression for Φ in (A-9) can be simplified using (3-51) and (3-52) with the approximations that $\mu = 0$ and $V_F = 0$, or

$$V_{C1}((m+d)T) \approx n d I_{on} \Psi R_L \qquad \text{(A-11)}$$

$$V_{Cj}((m+d)T) \approx n d I_{on} \Psi R_L + \frac{d T I_{on} \Psi}{C} \qquad \text{(A-12)}$$

This gives the expressions for Φ and t_{max} as

$$\Phi \approx \frac{n}{n-1} \cdot \frac{\tau_{2b}}{T} \qquad \text{(A-13)}$$

$$t_{max} \approx \tau_{2b} \ln\left(\frac{n-1}{n} \cdot \frac{T}{\tau_{2b}}\right) \qquad \text{(A-14)}$$

Using the approximations in Section 3.2, it is assumed that $t_{max} << \tau_{2a}$, so that

$$e^{\frac{-t_{max}}{\tau_{2a}}} \approx 1 - \frac{t_{max}}{\tau_{2a}} \tag{A-15}$$

Substituting (A-10)-(A-15) into (A-5) gives a simplified expression for the output ripple ΔV_o:

$$\Delta V_o \approx \frac{dTI_{on}\Psi(1-\alpha)}{C}[1 - \Phi(1 - \ln\Phi)] \tag{A-16}$$

APPENDIX B

DERIVATION OF THE SYSTEM TRANSFER FUNCTIONS

To derive the system transfer functions it is necessary to start with the state equation found in (3-33), or

$$\dot{x} = Ax + BU \tag{B-1}$$

where (B-1) is the state equation averaged over the entire switching period. For convenience, the input vector to state vector transfer function will be derived first.

Assume that a small variation in the input vector

$$u = U + \hat{u} \tag{B-2}$$

causes a similar variation in the state vector

$$x = X + \hat{x} \tag{B-3}$$

The duty cycle is assumed to remain constant, or $d = D$. Substitution into (B-1) gives

$$\dot{X} + \dot{\hat{x}} = A(X + \hat{x}) + B(U + \hat{u}) \tag{B-4}$$

The dynamic model can be extracted from (B-4) and, neglecting second-order terms, is given by

$$\dot{\hat{x}} = A\hat{x} + B\hat{u} \tag{B-5}$$

where A and B are defined in (3-44) and (3-45). Using Laplace transforms, the input vector to state vector transfer function can be shown to be

$$\frac{\hat{x}(s)}{\hat{u}(s)} = (sI - A)^{-1}B \tag{B-6}$$

Using (3-44) and (3-45), expanding (B-6) gives

$$\frac{\hat{x}(s)}{\hat{u}(s)} = \frac{\begin{bmatrix} s - A_{22} & A_{12} \\ A_{21} & s - A_{11} \end{bmatrix}\begin{bmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \end{bmatrix}}{|sI - A|} \tag{B-7}$$

where

$$|sI - A| = s^2 - (A_{11} + A_{22})s + A_{11}A_{22} - A_{21}A_{12} \tag{B-8}$$

Equation (B-8) can be factored and simplified using the approximations of Section 3.2, with the final result that

$$|sI - A| \approx \left(s + \frac{1}{kCR_L}\right)(s + 2\pi f_s \alpha(1 - \mu)) \tag{B-9}$$

The only transfer function of interest is the one relating the input current to the output voltage. Assuming that (3-54) holds, this is given by (B-7)-(B-9) as

$$\frac{\hat{v}_o(s)}{\hat{i}_{on}(s)} = G_c(s) \approx \frac{\frac{nD\Psi}{kC}(s+\omega_c)}{\left(s+\frac{\omega_c}{\omega_c(n-1+k)CR_L+1}\right)\left(s+\frac{\omega_c(n-1+k)CR_L+1}{kCR_L}\right)} \tag{B-10}$$

where

$$\omega_c \approx 2\pi f_s(1-\mu) \tag{B-11}$$

Upon examination of (B-10) it would appear that $G_c(s)$ is a second-order system with a zero in the numerator. However, in cases where $k >> n$ $G_c(s)$ can be approximated as a first-order function whose value is

$$G_c(s) \approx \frac{\frac{nD\Psi}{kC}}{\left(s+\frac{1}{kCR_L}\right)} \tag{B-12}$$

As would be expected, at zero frequency ($s = 0$) (B-12) reduces to

$$\frac{V_o}{I_{on}} = nD\Psi R_L \tag{B-13}$$

which is also given in (3-55).

As discussed in Chapter 5, to derive the duty cycle to state vector transfer function it is assumed that a small perturbation occurs

$$d = D + \hat{d} \tag{B-14}$$

while the input vector remains constant. Because matrices A and B are complicated functions of d, there is no way to easily factor out $\hat{d}$. Instead, the A and B matrices are expanded in a Taylor series about the steady-state value of the duty cycle, D. The Taylor series expansion of a function $g(d)$ about a point D is given by [41]

$$g(d) = \sum_{q=0}^{\infty} \frac{g^q(D)}{q!} \cdot (d-D)^q \tag{B-15}$$

This allows A and B to be written in the form:

$$A(d-D) = A(D) + a_1(D)(d-D) + (a_2(D)(d-D)^2 + \ldots) \tag{B-16}$$

$$B(d-D) = B(D) + b_1(D)(d-D) + (b_2(D)(d-D)^2 + \ldots) \tag{B-17}$$

Neglecting all terms higher than first-order, evaluation of (B-16) and (B-17) using (B-14) and substitution of (B-3) and (B-16)-(B-17) into (B-1) gives

$$\dot{X} + \dot{\hat{x}} \approx (A + a_1\hat{d})(X + \hat{x}) + (B + b_1\hat{d})U \tag{B-18}$$

where the first-order coefficient matrices, a_1 and b_1, are

$$a_1 = \begin{bmatrix} \frac{1}{kC}\left[\frac{M\Sigma(n-1)}{(R_{on}+R_{esr})} + \frac{(1-\alpha)(1-M)}{R_L}\right] & \frac{-M(n-1)}{kC(R_{on}+R_{esr})} \\ \frac{-1}{C}\left[\frac{M\Sigma}{(R_{on}+R_{esr})} + \frac{(1-M)}{(n-1+k)R_L}\right] & \frac{M}{C(R_{on}+R_{esr})} \end{bmatrix} \tag{5-19}$$

$$b_1 = \begin{bmatrix} \frac{\Psi}{kC}\left[n - M(n-1) - \frac{MDT(n-1)}{\alpha C(R_{on} + R_{esr})}\right] & \frac{M(n-1)}{k\alpha C(R_{on} + R_{esr})} \\ \frac{M\Psi}{C}\left[1 + \frac{DT}{\alpha C(R_{on} + R_{esr})}\right] & \frac{-M}{C(R_{on} + R_{esr})} \end{bmatrix} \tag{5-20}$$

where M and Σ are μ and σ evaluated at $d = D$.

The dynamic model can be extracted from (B-18) and, neglecting second-order terms, is given by

$$\dot{\hat{x}} \approx A\hat{x} + \hat{d}(a_1 X + b_1 U) \tag{B-21}$$

Using Laplace transforms, the duty cycle to state vector transfer function can be shown to be

$$\frac{\hat{x}(s)}{\hat{d}(s)} \approx (sI - A)^{-1}(a_1 X + b_1 U) \tag{B-22}$$

Again, the only transfer function of interest is the one relating the duty cycle to the output voltage. Assuming that (3-54) holds, this transfer function can be shown to be

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = G_d(s) \approx \frac{Y_1(s - A_{22}) + Y_2 A_{12}}{\left(s + \frac{\omega_c}{\omega_c(n-1+k)CR_L + 1}\right)\left(s + \frac{\omega_c(n-1+k)CR_L + 1}{kCR_L}\right)} \tag{B-23}$$

where

$$Y_1 = a_{11}V_o + a_{12}V_{Cj}(mT) + b_{11}I_{on} + b_{12}V_F \tag{B-24}$$

$$Y_2 = a_{21}V_o + a_{22}V_{Cj}(mT) + b_{21}I_{on} + b_{22}V_F \tag{B-25}$$

$$\omega_d \approx 2\pi f_s \alpha(1-\mu) - 2\pi f_s(1-\alpha)(1-\mu)\cdot\frac{Y_2}{Y_1} \tag{B-26}$$

Again, $G_d(s)$ appears to be a second-order system with a zero in the numerator. However, if V_o is given by (3-55) and $V_{Cj}(mT)$ is approximated from (3-48) as

$$V_{Cj}(mT) \approx V_o + V_F \quad ; \quad \mu = 0 \tag{B-27}$$

then for $k >> n$ (B-24) and (B-25) can be approximated as

$$Y_1 \approx \frac{\mu\Psi I_{on}}{C}\cdot\frac{n}{k} \tag{B-28}$$

$$Y_2 \approx \frac{\mu\Psi I_{on}}{C}\left(1+\frac{dT}{\tau_{2b}}\right) \tag{B-29}$$

This gives the value of (B-26) to be

$$\omega_d \approx (2\pi f_s\alpha(1-\mu))\left[1+\frac{\mu(n-1)}{n}\cdot\left(1+\frac{dT}{\tau_{2b}}\right)\right] \approx 2\pi f_s(1-\mu) \tag{B-30}$$

The result is that $G_d(s)$ can be approximated as a first-order function whose value is

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = G_d(s) \approx \frac{1}{\left(s+\frac{1}{kCR_L}\right)}\cdot\frac{nI_{on}\Psi}{kC} \tag{B-31}$$

As would be expected, at zero frequency ($s = 0$) (B-31) reduces to

$$\frac{V_o}{D} = n\Psi I_{on} R_L \tag{B-32}$$

which is also given in (3-55).

APPENDIX C

DERIVATION OF THE STANDARD PARAMETER MODELS

The standard parameter models for the capacitors, power MOSFETs, and diodes were derived from data obtained from the databooks of the AVX Corporation, Motorola, Inc., International Rectifier, and General Instrument Corporation, respectively.

C.1. Capacitors

The SupraCap^{TM} capacitors come in three different dielectrics: C0G, X7R, and Z5U. The Z5U dielectric was chosen because it has the highest capacitance per unit volume. The SupraCap^{TM} capacitors come in six different package styles: SM-1, SM-2, SM-3, SM-4, SM-5, and SM-6. The volume of each package, along with the maximum capacitance available at the different working voltages, and the capacitance per unit volume are given in Table C-1.

The dependence of the capacitance per unit volume on the working voltage appears to be an inverse relationship of the type

$$S(V_{wk}) = \frac{k_c}{V_{wk}} \tag{C-1}$$

where k_c is a constant. Table C-2 shows the relationship between S and V_{wk}. The average value of k_c is determined to be 24188, and $k_c = 24000$ was used in the design procedure.

Table C-1: Capacitance per unit volume for SupraCap capacitors as a function of working voltage.

Package Style	Volume (in^3)	Maximum $\mu F / in^3$ @ 50V	Maximum $\mu F / in^3$ @ 100V	Maximum $\mu F / in^3$ @ 200V
SM-1	0.728	576.9	219.8	82.4
SM-2	0.933	632.4	246.5	64.3
SM-3	0.373	536.2	201.1	80.4
SM-4	0.125	480	184.0	120.0
SM-5	0.053	434.0	169.8	71.7
SM-6	1.965	661.6	366.4	234.1
	Average	553.5	231.3	108.8

Table C-2: Average capacitance per unit volume for SupraCap capacitors as a function of working voltage.

S - $\mu F / in^3$	V_{wk} - volts	k_c
553.5	50	27675
231.3	100	23130
108.8	200	21760
	Average	24188

The relationship between C and R_{esr} was found using a 5.6 μF capacitor where R_{esr} = 1 mΩ and a 24 μF capacitor where R_{esr} = 4 mΩ. This gives

$$R_{esr} \approx \frac{24\text{m}\Omega\text{-}\mu\text{F}}{C} \tag{C-2}$$

C.2. Power MOSFETs

In this section the standard model is derived for the switching power MOSFETs M_2-M_n and the current source power MOSFET M_C.

C.2.1. Switching MOSFETs

The parameters of interest for the switching power MOSFETs M_2-M_n are R_{on}, C_{dso}, C_{dgo}, and C_{gso}. The relationship between R_{on} and V_{block} is given as [34]

$$R_{on}A_d \approx 3\times10^{-7}(V_{block})^{2.5} \tag{C-3}$$

where A_d is the power MOSFET drain area. The data in Table C-3 was obtained from [36], and shows the relationship between V_{block}, R_{on} and I_d. The area is calculated using (C-3), and is normalized to 1 amp. This allows (C-3) to be rewritten as

$$R_{on} \approx \frac{3\times10^{-7}(V_{block})^{2.5}}{I_d A_{dnorm}} \tag{C-4}$$

The relationship between A_{dnorm} and V_{block} can be determined to be

$$A_{dnorm} \approx 2.65\times10^{-6}(V_{block})^2 \tag{C-5}$$

which allows (C-4) to be rewritten as

$$R_{on} \approx \frac{0.1132(V_{block})^{0.5}}{I_d} \tag{C-6}$$

Table C-3: The power MOSFET relationship between V_{block}, R_{on}, I_d, and A_{dnorm}.

Device	V_{block} (volts)	R_{on} (ohms)	I_d (amps)	A_{dnorm}
MTM1M100	1000	10	0.5	1.9
MTM2N90	900	8	1.0	0.91
MTM3N80	800	7	1.5	0.52
MTM3N60	600	2.5	1.5	0.315
MTM2N50	500	4	1	0.419
MTM5N40	400	1	2.5	0.32
MTM8N20	200	0.4	4	0.106
MTM12N10	100	0.18	6	0.028
MTM12N05	50	0.2	6	0.004

The relationship between the zero-bias parasitic capacitance values, V_{block} and R_{on} was found using the data from Table C-4. This relationship was assumed to be an inverse relationship of the form

$$C = \frac{k_c(V_{block})}{R_{on}} \tag{C-7}$$

where k_c is again a constant and is a function of V_{block}. The values of k_c for the gate-source, drain-source, and drain-gate capacitances are given by

$$k_c = 1.1 V_{block} + 33 \tag{C-8}$$

$$k_c = 1.17 V_{block} + 147 \quad \text{(C-9)}$$

$$k_c = 0.85 V_{block} + 81 \quad \text{(C-10)}$$

respectively, where k_c has units of pF/Ω.

Table C-4: The MOSFET relationship between V_{block}, R_{on}, and the parasitic capacitances.

Device	V_{block} (volts)	R_{on} (ohms)	C_{gso} (pF)	C_{dso} (pF)	C_{dgo} (pF)
MTM12N05	50	0.2	300	1170	590
MTM35N05	50	0.055	1600	6400	2300
MTM45N05	50	0.035	2600	6400	2300
MTM60N05	50	0.028	4000	8800	5900
MTM12N10	50	0.18	700	1800	600
MTM20N10	100	0.15	1000	2300	1200
MTM25N10	100	0.075	1600	2300	6400
MTM55N10	100	0.04	4000	8800	5900
MTM8N20	200	0.4	700	1200	600
MTM15N20	200	0.16	1800	2900	1200
IRF240	200	0.18	1300	2600	1800
IRF250	200	0.085	2500	4100	2900

C.2.2. Current Source Power MOSFET

The parameters of interest for M_C are g_m, V_T, and I_{Mcmax}. The relationship of g_m to I_d was determined to be a linear relationship of the form

$$g_m = k_c I_d \tag{C-11}$$

where k_c is again a constant. Using the data in Table C-5, the value of k_c is found to be 0.53. Therefore, (C-11) can be rewritten as

$$g_m = I_d \cdot \frac{0.53 \text{ mhos}}{\text{A}} \quad ; \quad I_d \geq 0.94 \text{ A} \tag{C-12}$$

$$g_m = 0.5 \text{ mhos} \quad ; \quad I_d < 0.94 \text{ A} \tag{C-13}$$

The threshold voltage V_T was found to be approximately the same (-3.5 V) for all devices listed in the databooks.

Table C-5: The power MOSFET relationship of g_m and I_d.

V_{block} (volts)	I_d (amps)	g_m (mhos)	k_c
50	6	2	0.33
50	10	5	0.5
50	12.5	6	0.48
100	4	2	0.5
100	6	2	0.33
100	10	5	0.5
250	1.5	1	0.67
250	2.5	2	0.8
250	4	3	0.75
500	1	0.5	0.5
		Average	0.53

The relationship of I_{Mcmax} to V_{block} was found to be an inverse relationship of the form

$$I_{Mcmax} = \frac{k_c}{V_{block}} \tag{C-14}$$

where k_c is a constant. Using the data in Table C-6, the value for k_c was found to be approximately 3000. This allows (C-14) to be rewritten as

$$I_{Mcmax} = \frac{3000 \text{ V- A}}{V_{block}} \tag{C-15}$$

Table C-6: The power MOSFET relationship between I_{Mcmax} and V_{block}.

V_{block} (volts)	I_{Mcmax} (amps)	k_c
1000	3	3000
900	4	3600
600	6	3600
500	8	4000
400	10	4000
200	15	3000
100	25	2500
50	60	3000
	Average	3000

C.3. Diodes

The data for the standard power diode model was taken from [13] and [21]. The parameters of interest are V_F, C_{jo}, and I_{dmax} as a function of I_{diode} and V_{block}. These relationships were found using the data in Table C-7 for the low-voltage diodes and Table C-8 for the high-voltage diodes. The results are given as

$$V_F = k_T[\ln((I_{on}) + \ln(10)(0.0206 V_{block} + 7.22))] \tag{6-16}$$

$$C_{jo} = 6528 - 6.28 V_{block} \tag{6-17}$$

$$I_{dmax} = 49.6 - 0.046 V_{block} \tag{6-18}$$

where $k_T = 0.0259$ at $T_j = 25°C$ and $k_T = 0.0302$ at $T_j = 75°C$.

Table C-7: Low-voltage power diode parameters.

V_{block} (volts)	I_{diode} (amps)	C_{jo} (pF)
50	1.1	165
50	5.5	500
50	8	2500
50	30	5100
50	60	7200
100	1.1	97
100	3.3	165
100	5.5	275
100	8	1400
100	15	1700
100	30	3900
100	45	3900

Table C-8: High-voltage power diode parameters.

V_{block} (volts)	I_{diode} (amps)	C_{jo} (pF)
600	0.5	38
600	1	38
600	2	100
600	3	100
600	8	138
600	15	370
600	22	1640
600	25	1640
1000	1	38
1000	3	125
1000	6	230

APPENDIX D

DESIGN PROCEDURE SOURCE LISTING

This is the source listing for the design procedure, written in Turbo C++. Comments have been included to enable the reader to modify the source code to change such parameters as the junction temperature, the component models, and other parameters of interest.

```
/*design.c*/

/*This file is used to design a switched-capacitor dc-dc converter for a minimum total capacitance given
the input voltage, output voltage, percent ripple, output power and minimum efficiency.*/

/*Define constants*/

#define VDIODE .3 /*initial diode voltage*/
#define VLIN 10.0 /*gate voltage swing above ground*/
#define NMAX 15 /*maximum number of stages program will handle*/
#define RONDEC .01 /*increment for Ron*/
#define CINC 1e-8 /*increment for C*/
#define ESR 24e-9 /*conversion factor, product of Resr times C*/
#define S .024  /*constant to convert capacitance to inches cubed*/
#define FDEC 1000  /*factor to decrement frequency*/
#define FMAX 1e6 /*maximum switching frequency*/
#define VT -3.5 /*Threshold voltage of Mc*/
#define PHI .75 /*p-n potential*/
#define KT .0302 /*constant at T=75 degrees C*/
#define PI 3.14 /*value of pi*/
#define PRI .1 /*power dissipation of Ri*/
#define PHASEM 60.0 /*value of phase margin*/
#define K 1.0 /*initial value of k*/
#define VBMAX 1000 /*maximum blocking voltage*/
#define VBMIN 50 /*minimum blocking voltage*/
#define VWORKMAX 200.0 /*maximum capacitor working voltage*/
#define GMMIN .5 /*minimum value for gm*/
#define MARGIN 1.25 /*safety margin for blocking and working voltages*/
#include <stdio.h>
#include <math.h>

void main (void)
{
int i, npoint, kflag;
double n, Vin, Vout, Pout, Vdmax, psi, percent, nstages, d, Cmin, Ron, Resr, vf, T, RL, Ion;
double f, C, Rp, k, Rx, Ry, R1, Vwork, v2dmax, detA, L1, T1, L2a, T2a, L2b, T2b, Ctotal;
```

```
double theta, Gamma, gamma, sigma, mu, Imc, Ronmax, c11, c12, e21, e22, a11, a12, a21, a22, u11, u21;
double v1c, v1d, v2c, v2d, vx, Vsource, etamax, Volume, tmax1, tmax2, tmax, Vtmax1, Vtmax2, vflag;
double ripple, gm, VM[NMAX], VB[NMAX], Es, Ea[NMAX], Eb[NMAX];
double Ps, fmax, nmax, fflag, Iratingmin, Cjo, vlin, Id, Irating, Ronmin, Eds[NMAX], Edg[NMAX]
double DVc, Vgate, Vb, eta, Egs[NMAX], Ecgd, Ecsd, Ecsg, Vt, test1, test2, test3, test4;
double Crss, Ciss, Coss, Cgso, Cdso, Cdgo, Pta[NMAX], Ptb[NMAX], Ptm[NMAX], Ptmc;
double Ron25, Imj, Isat, Imaxm, Imaxd, Imax, crossover, phasem, omegaz, omegap, vref, gain, Homega;
double Ri, Rb, Rf, Cf1, Cf2, flag, etamin, Volumek, margin;
char string[20];
/*_____________________________________________________________________*/
/*get the input parameters*/
clrscr ();
margin = MARGIN;
printf ("Enter the input voltage: ");
gets (string);
Vin = atof(string);
Vb = margin*Vin;
if (Vb>VBMAX)
    {
    printf ("\n\nVin is too large - No solution!!!\n\n");
    return;
    }
if (Vb<VBMIN)
    Vb = VBMIN;
printf ("Enter the output voltage: ");
gets (string);
Vout = atof(string);
printf ("Enter the percent ripple: ");
gets (string);
percent = atof(string);
printf ("Enter the output power:  ");
gets (string);
Pout = atof(string);
/*compute the number of stages*/
nstages = (Vin+VDIODE)/(Vout+VDIODE);
nmax = floor(nstages);
n = nmax;
printf ("Enter the minimum efficiency in percent: ");
gets (string);
etamin = atof(string);
n = 2;
while (1)               /*loop to determine minimum n*/
    {
    etamax = n*Vout/Vin*100;
    if ((etamax-etamin)>0)
        break;
    else
        n++;
    }
```

```
/*compute maximum current*/
Imaxm = 3000.0/Vb;          /*max mosfet current*/
Imaxd = 49.6-.046*Vb        /*max diode current*/
if (Imaxd>Imaxm)
    Imax = Imaxm;
else
    Imax = Imaxd;
Volumek = 1e6;
k = K;
kflag = 0;
while (1)  /*loop to determine the minimum volume using k*/
    {
    vflag = 0;
    Volume = 1e6;
    while (1)  /*loop to determine minimum volume using n*/
        {
        npoint = (int)(n);/*integer number of stages*/
/*compute circuit parameters*/
        RL = Vout*Vout/Pout;      /*load resistance*/
        d = 1/n;                  /*duty cycle*/
        Ion = sqrt(Pout/RL);      /*charging current*/
        if (Ion>Imax)
            {
            printf ("\n\nIon is too large - No solution!!!\n\n");
            return;
            }
/*compute Mc and Mj parameters*/
        Vt = VT;
        if(Ion<=1.0)
            gm = GMMIN;
        else
            gm = .53*Ion;
        vlin = VLIN;
        Imc = Ion;
        Imj = (1-d)*Ion/(n-1);
        Iratingmin = 40.0/sqrt(Vb);
        if (Imj<Iratingmin)
            Irating = Iratingmin;
        else
            Irating = Imj;
        Ronmin = (4e-6*Vb*Vb+.018)*1.45;
        Ronmax = 1.45*(3e-7*pow(Vb,1.5))/(Irating*(4.627e-10*Vb*Vb+1.43e-6*Vb+7.345e-6));
        Ron = Ronmax;
        Ron25 = Ron/1.45;
/*compute diode parameters*/
        Cjo = (6528-6.28*Vb)*1e-12;
        vf = KT*(log(Ion)+log(10)*(.0206*Vb+7.22));
/*maximum drain voltage on Mc and maximum discharge initial condition*/
        Vdmax = Vin-Ion/gm-.1;
```

```
        v2dmax = (Vdmax-Vout)/(n-1)-vf;
/*set frequency to maximum value*/
        fmax = FMAX;
        f = fmax;
/*compute the minimum switching frequency*/
        while (1)    /*loop to compute minimum switching frequency*/
            {
            T = 1/f;
            fflag = 0;
/*compute minimum value for charging capacitance Cmin
 and compute the value for Resr*/
            Cmin = (d*T*Ion)/(v2dmax-Vout-vf);
            if (Cmin<=0)
                {
                printf ("\n\nCmin is negative - There is no solution!!!\n\n");
                return;
                }
            C = Cmin;
            Resr = ESR/C;
            R1 = Resr/k;
            Ry = RL+R1;
            while (1)      /*loop to determine the minimum value for C*/
                {
                while (1)      /*loop to determine maximum value for Ron*/
                    {
/*compute initial conditions*/
                    Rp = (Ron+Resr)/(n-1);
                    Rx = RL+Rp;
                    L1 = 1/(k*Ry*C);
                    T1 = 1/L1;
                    L2a = 1/(RL*C*(n-1+k)+Rp*(n-1)*C+k*C*R1);
                    T2a = 1/L2a;
                    L2b = T2a/(C*C*k*(n-1)*(R1*Rp+RL*Rp+R1*RL));
                    T2b = 1/L2b;
                    Gamma = (L2a*L2b)/(L2b-L2a);
                    mu = exp(-(1-d)*T/T2b);
                    theta = T2a*exp(-(1-d)*T/T2a)-T2b*mu;
                    gamma = exp(-(1-d)*T/T2a)-mu;
                    sigma = exp(-d*T/T1);
                    e11 = theta-(n-1)*C*Rx*gamma;
                    e12 = (n-1)*C*RL*gamma;
                    e21 = k*C*RL*gamma;
                    e22 = theta-k*C*Ry*gamma;
                    a11 = (Gamma*e11*sigma-1)/T;
                    a12 = Gamma*e12/T;
                    a21 = Gamma*e21*sigma/T;
                    a22 = (Gamma*e22-1)/T;
                    u21 = (Ion*d*Gamma)/C*(e21/k+e22)+(vf*(1-Gamma*e22))/T;
                    u11 = (Ion*d*Gamma)/C*(e11/k+e12)-(vf*Gamma*e12)/T;
```

```
                detA = (a11*a22)-(a12*a21);
                v1c = (a12*u21-a22*u11)/detA;
                v1d = sigma*v1c+(d*T*Ion)/(k*C);
                v2c = (a21*u11-a11*u21)/detA;
                v2d = v2c+(d*T*Ion)/C;
                vx = v2d-vf;
    /*check if capacitor working voltage is exceeded*/
                Vwork = v2d*margin;
                if (Vwork>VWORKMAX)
                    {
                    printf ("\n\nVwork is too large - No solution!!!\n\n");
                    return;
                    }
    /*_____*/
    /*compute switching loss*/
                Ron25 = Ron/1.45;
                Cgso = 1e-12*(1.1*Vb+33)/Ron25;
                Cdso = 1e-12*(1.17*Vb+147)/Ron25;
                Cdgo = 1e-12*(.85*Vb+81)/Ron25;
                for (i=2; i<(n+1); i++)
                    VM[i] = Vout+(i-1)*(vf+v2d);
                if (VM[npoint]+Imc/gm<=Vin)
                    {
                    for (i=2; i<(n+1); i++)
                        VB[i] = Vout+(i-1)*vf+(i-2)*v2d;
                        Vgate = Vin-Imc/gm+Vt;
                        DVc = (n-1)*d*T*Ion/C;
                        test1 = Vin-VM[npoint];
                        test2 = sqrt(1+test1/PHI);
                        Ecgd = 4/3*Cdgo*PHI*(sqrt(test2*(test1-2*PHI)+2*PHI)+Cdgo*((Vin-
Vgate)*(Vin-Vgate)));
                        if (Ecgd<0)
                            Ecgd = -Ecgd;
                        test1 = Vin-VM[npoint];
                        test2 = sqrt(1+test1/PHI);
                        test3 = test1-DVc;
                        Ecsd = 4/3*Cdso*PHI*(test2*(test1-2*PHI))+Cdso*test3*test3;
                        if (Ecsd<0)
                            Ecsd = -Ecsd;
                        Ecsg = Cgso*((Vin-Vgate)*(Vin-Vgate));
                        for (i=2; i<(n+1); i++)
                            {
                            Ea[i] = 4/3*Cjo*PHI*(sqrt(1+v2d/PHI)*(v2d-2*PHI)+2*PHI);
                            Eb[i] = 4/3*Cjo*PHI*(sqrt(1+VB[i]/PHI)*(VB[i]-2*PHI)+2*PHI);
                            Eds[i] = 4/3*Cdso*PHI*(sqrt(1+(VM[i]-Vout)/PHI)*(VM[i]-Vout-
2*PHI)+2*PHI);
                            Edg[i] = 4/3*Cdgo*PHI*(sqrt(1+VM[i]/PHI)*(VM[i]-
2*PHI)+2*PHI)+Cdgo*(Vout*Vout+vlin*vlin);
                        Egs[i] = Cgso*(Vout*Vout+vlin*vlin);
```

```
                    }
                Es = (Ecgd+Ecsd)/2;
                for (i=2; i<(n+1); i++)
                    Es = Es+Ea[i]+Eb[i]+Eds[i]+Edg[i]/2+Egs[i]/2;
                Ps = Es*f;
                psi = sqrt(Pout/(Pout+Ps));
                Imc = sqrt(Pout/(psi*psi*RL));
                if (Imc>Imax)
                    {
                    fflag = 1;
                    break;
                    }
/*see if Vsource<Vin, stop when true*/
                if(Imc<=1.0)
                    gm = GMMIN;
                else
                    gm = .53*Imc;
                Vsource = (n-1)*(v2d+vf)+Vout+Imc/gm;
                if (Vsource<Vin)
                    break;
                else
                    {
                    Ron = Ron-RONDEC;
                    if (Ron<Ronmin)
                        {
                        Ron = Ronmax;
                        C = C+CINC;
                        Resr = ESR/C;
                        R1 = Resr/k;
                        Ry = RL+R1;
                        }
                    }
            }
        else
            {
            Ron = Ron-RONDEC;
            if (Ron<Ronmin)
                break;
            }
        }           /*end of Ron loop*/
/*_____________________________________________________________________*/
/*compute ripple*/
        if (fflag==1)
            break;
        if (Ron>Ronmin)
            {
            tmax1 = (v1d*(T2a-((n-1)*C*Rx))+vx*(n-1)*C*RL)*T2b;
            tmax2 = (v1d*(T2b-((n-1)*C*Rx))+vx*(n-1)*C*RL)*T2a;
            tmax = -(T2a*T2b)/(T2a-T2b)*log(tmax1/tmax2);
```

```
                Vtmax1 = Gamma*exp(-L2a*tmax)*(v1d*(T2a-((n-1)*C*Rx))+(vx*(n-1)*C*RL));
                Vtmax2 = Gamma*exp(-L2b*tmax)*(-v1d*(T2b-((n-1)*C*Rx))-(vx*(n-1)*C*RL));
                ripple = Vtmax1+Vtmax2-v1c;
/*Determine if ripple is less than desired*/
                if (ripple<=(Vout*percent*.01))
                    break;
                else
                    {
                    C = C+CINC;
                    Resr = ESR/C;
                    R1 = Resr/k;
                    Ry = RL+R1;
                Ron = Ronmax;
                    Imc = Ion;
                    }
                }
            else
                {
                C = C+CINC;
                Resr = ESR/C;
                R1 = Resr/k;
                Ry = RL+R1;
                Ron = Ronmax;
                }
            }       /*end of C loop*/
        if (fflag==1)
            f = f-FDEC;
            if (f<=0)
                {
                printf ("\n\nFrequency went to zero - No solution!!!\n\n");
                return;
                }
        else
            {
            eta = n*psi*Vout/Vin*100;
            if (eta>etamin)
                break;
            else
                {
                f = f-FDEC;
                if (f<=0)
                    {
                    printf ("\n\nFrequency went to zero - No solution!!!\n\n");
                    return;
                    }
                }
            }
        }       /*end of frequency loop*/
/*Program has calculated the maximum values for Ron and C.
```

```
The total capacitance, volume and efficiency are found. */
        Ctotal = (n-1+k)*C;
        if (vflag==1)
        break;
        if ((Ctotal*Vwork/S)<Volume)
            {
            Volume = Ctotal*Vwork/S;
            n++;
            if (n>nmax)
                {
                n--;
                break;
                }
            }
        else
            {
            vflag = 1;
            n--;
            if (n==1.0)
            n = 2.0;
            }
        }           /*end of minimum volume n loop*/
    if (kflag==1)
            break;
    if (Volume<Volumek)
        {
        Volumek = Volume;
        k = k+1.0;
        }
    else
        {
        k = k-1.0;
        kflag = 1;
        }
    }           /*end of minimum volume k loop*/
/*_____________________________________________________________________*/
/*The thermal parameters are computed.*/
for (i=2; i<(n+1); i++)
    {
    Pta[i] = d*Ion*vf+f*Ea[i];
    Ptb[i] = Imj*vf+f*Eb[i];
    Ptm[i] = Imj*(v2c-Vout+DVc/(2*(n-1)))+f*(Edg[i]+Egs[i]+Eds[i]);
    }
Ptmc = d*Imc*(Vin-(2*VM[npoint]-DVc)/2)+f*(Ecsd+Ecgd+Ecsg);
/*_____________________________________________________________________*/
/*Compute mosfet input, output, and reverse transfer capacitances*/
Ciss = Cgso+Cdgo/5.86;
Coss = (Cdgo+Cdso)/5.86;
Crss = Cdgo/5.86;
```

```
Irating = 1.45*(3e-7*pow(Vb,1.5))/(Ron25*(4.627e-10*Vb*Vb+1.43e-6*Vb+7.345e-6));
if (Irating<Iratingmin)
    Irating = Iratingmin;
/*_____________________________________________________________________*/
/*Output results to screen*/
clrscr ();
printf ("\nThe number of stages is %.0f\n", n);
printf ("Efficiency is %3.1f%\n", eta);
printf ("The output ripple is %4.3f volts\n", ripple);
printf ("The switching frequency is %6.0f Hz\n", f);
printf ("C is %.2e farads\n", C);
printf ("The working voltage is %4.1f volts\n", Vwork);
printf ("Resr is %4.4f ohms\n", Resr);
printf ("Ctotal is %.2e farads\n", Ctotal);
printf ("The capacitor volume is %.4e cubic inches\n", Volume);
printf ("Ron(75)is %5.3f ohms\n", Ron);
printf ("Ron(25)is %5.3f ohms\n", Ron25);
printf ("The current rating of Mj is %4.2f amps\n", Irating);
printf ("The mosfet Ciss is %.1e farads\n", Ciss);
printf ("The mosfet Coss is %.1e farads\n", Coss);
printf ("The mosfet Crss is %.1e farads\n", Crss);
printf ("The power dissipation of Mj is %5.3f watts\n", Ptm[npoint]);
printf ("The average current through Mc is %5.3f amps\n", d*Imc);
printf ("The transconductance of Mc is %5.2f mhos\n", gm);
printf ("The power dissipation of Mc is %5.2f watts\n", Ptmc);
printf ("The average diode current is %5.3f amps\n", d*Ion);
printf ("The diode capacitance is %.2e farads\n", Cjo);
printf ("The A diode power dissipation is %5.3f watts\n", Pta[npoint]);
printf ("The B diode power dissipation is %5.3f watts\n", Ptb[npoint]);
/*_____________________________________________________________________*/
/*calculate the dynamic parameters*/
crossover = f/3*2*PI;
phasem = PHASEM*PI/180.0;
omegaz = -crossover/tan(phasem+PI/2);
omegap = -crossover*tan(phasem+PI/2);
printf ("Enter the reference voltage: ");
gets (string);
vref = atof (string);
printf ("Enter 1 for current control, enter 2 for duty cycle control: ");
gets (string);
flag = atof (string);
if (flag==1)
    {
    printf ("Enter the gain of the gate drive circuit: ");
    gets (string);
    gain = atof (string);
    Homega = k*C*sqrt (crossover*crossover+1/(k*C*RL*k*C*RL))/(psi*gm*gain);
    }
if (flag==2)
```

```
    {
    printf ("Enter the gain of the PWM circuit: ");
    gets (string);
    gain = atof (string);
    Homega = k*C*sqrt (crossover*crossover+1/(k*C*RL*k*C*RL))/(n*Imc*psi*gain);
    }
Ri = (Vout-vref)*(Vout-vref)/PRI;
Rb = Ri/(Vout/vref-1);
Rf = Homega*Ri;
Cf1 = 1/(Rf*omegaz);
Cf2 = 1/(Rf*omegap);
printf ("Ri is %6.0f ohms\n", Ri);
printf ("Rb is %6.0f ohms\n", Rb);
printf ("Rf is %6.0f ohms\n", Rf);
printf ("Cf1 is %.3e farads\n", Cf1);
printf ("Cf2 is %.3e farads\n", Cf2);
printf ("The crossover frequency is %6.0f Hz\n", crossover/(2*PI));
}
```

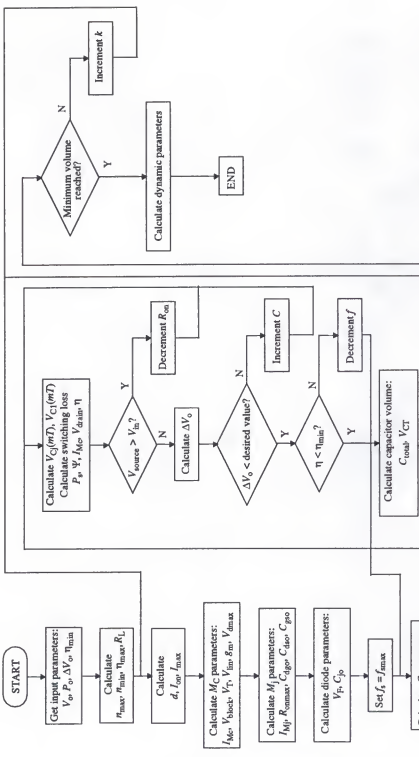


Figure D-1. Flowchart of the optimized design procedure.

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BIOGRAPHICAL SKETCH

After graduating with high honors in 1974 from Niceville High School in Niceville, Florida, *William Scott Harris* studied electrical engineering at Auburn University in Auburn, Alabama. He graduated with highest honors in 1978, and went to work at Eglin Air Force Base, Florida, for the United States Air Force as a civilian electrical engineer. While at Eglin, his job responsibilities included the design of hardware and software used in electronic instrumentation systems for both range and airborne applications. In 1988 *Mr. Harris* graduated from the University of West Florida in Pensacola with a Master of Science degree in systems analysis. In 1991 he was selected by the Air Force to attend the University of Florida in Gainesville for the purpose of obtaining a Ph.D. in electrical engineering.

Mr. Harris lives in Niceville with his wife *Betsy* and their three children *Meg*, *Alex*, and *Abby*. He continues to work at Eglin Air Force Base for the United States Air Force as a civilian electrical engineer. *Mr. Harris* and his wife also own and operate the Harris Center for Learning, a preschool/tutoring business in Niceville.

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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